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FY-85 REPORT

MODTEQ, AN/FRC-170(V),

EQUALIZATION, AND CHANNEL MEDIUM

SIMULATIONS

Contract No. DCA 100-81-G-0001

January 1986

Prepared By

Technical Computing Center
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Prepared For

Defense Communications Agency
Defense Communications Engineering Center
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This report documents the hybrid simulations of LOS Selective Fading Channel Model, AN/FRC-170(V), Modulation Techniques and Hybrid Equalization, designed and maintained by Martin Marietta Aerospace in Orlando, Florida. Areas of special interest to this report are tasks 1 through 4 outlined in statement of work R220-85-011 as part of contract number DCA 100-81-G-0001. Those tasks include maintenance and modufication to the existing hybrid simulation of the AN/FRC-170(V) DRAMA radio, modifications, additions, and enhancements to the Advanced Modulation Techniques simulation study, and development of software systems to control and monitor the various simulation models.

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FORWARD

This report documents the hybrid simulations of LOS Selective Fading Channel Model, AN/FRC-170(V), Modulation Techniques and Hybrid Equalization, designed and maintained by Martin Marietta Aerospace in Orlando, Florida. Areas of special interest to this report are tasks 1 through 4 outlined in statement of work R220-85-011 as part of contract number DCA 100-81-G-0001. Those tasks include maintenance and modification to the existing hybrid simulation of the AN/FRC-170(V) DRAMA radio, modifications, additions, and enhancements to the Advanced Modulation Techniques simulation study, and development of software systems to control and monitor the various simulation models.

Provisions of this contract included the placement of a hybrid computer remote terminal (telephone modem, terminal with hardcopy unit, and stripchart recorder) at the Defense Communication Engineering Center. This terminal was used by the center's engineers to control the simulator, test the system under simulated channel effects, and extract system performance data.

The title on the front cover is correct.
Per Dr. Smith, DCEC/Code R220

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1. INTRODUCTION

This report discusses and documents the progress within the Martin Marietta Corporation Technical Computing Center of the Orlando Aerospace Division that pertains to the last 12 months, (FY-85) of a 24 month hybrid computer simulation study of the dual diversity AN/FRC-170(V) radio, line-of-sight, (LOS), frequency selective fading channel model, and advanced modulation techniques (MODTEQ).

The present simulation has taken advantage of models, simulations, and results of previous contracts DCA 100-81-C-0016, DCA 100-79-C-0048, and DCA 100-77-C-0061, and includes enhancements outlined as tasks 1 through 4 in statement of work R220-85-011 as part of contract number DCA 100-81-G-0001. These tasks will briefly be outlined here and delineated in Section 2. Included in Section 2 are references to more detailed discussions of work performed on the various tasks throughout the report.

Of the 8 tasks outlined in statement of work R220-85-011, tasks 1 through 4 are pertinent to the FY-85 effort and the last four (5 through 8) pertain to the FY-86 effort.

o Task 1 requires the maintenance of an accurate simulation of the DRAMA radio and frequency selective LOS fading channel model, using as a baseline the hybrid computer models developed previously under contracts 100-77-C-0061, 100-79-C-0048, 100-81-C-0016, and 100-83-C-0016. Additionally, any modifications to the pseudo error monitor, the baseband equalizer, and or the TDM framing alogrithm of the fielded radios were required to be reflected in the simulstion models to accomodate DCEC evaluations of these modifications.

o Task 2 requires the addition of a Nakagami-Rice fading channel model to allow DCEC engineers to study several LOS links by varying the multipath occurence factor.

o Task 3 requires that contractor add to the simulation, the following advanced modulation schemes at bandwidths and data rates shown:

1

o   QAM 16 level at 45 Mb/s with 14 Mhz BW

o   QAM 64 level at 90 Mb/s with 21Mhz BW, and
         135 Mb/s with 28 Mhz BW

o   PSK 8 level at 45 Mb/s with 14 and 21 Mhz BW

o   QPR 49 level at 45 Mb/s with 14 Mhz BW and 90
         Mb/s with 21 Mhz BW

Additional requirements include the capability to allow the DCEC engineer to vary the baseband filter rolloff ($\alpha=1$, $\alpha=.5$, $\alpha=.3$) for each of the data rates, modulation schemes, and bandwidths indicated above.

o Task 4 defines the simulation interactive terminal displays and controls provided by the contractor at DCEC in order to accomodate DCEC control of the simulation with references to both software and hardware necessary for remote control and analysis of results.

Section 2 explains the simulation models used in the transmitter and receiver. Enhancements such as the baseband equalizer, IF equalizer, and time division multiplexer are described in Section 3. Section 4 is an explanation of the LOS frequency selective channel model. Section 5 is an explanation of the work done on the advanced digital modulation techniques. Section 6 is a more detailed reference to the work performed in reference to the tasks outlined in the statement of work. Section 7 describes the user program. Section 8 is a brief description of the Technical Computing center at Martin Marietta Corporation where the AN/FRC-170(V) radio, MODTEQ, and related items are simulated.

2. DELINEATION OF TASKS

TASK #1

The DRAMA simulation of the AN/FRC-170(V) radio, including the frequency selective fading LOS radio channel, has been available for use by DCEC engineers. The simulation was prepared, when requested, numerous times through the year.

No modifications were made to the pseudo-error monitor, the baseband equalizer, or the TDM framing alogrithm of the fielded radio; therefore, no modifications of these subsystems were necessary on the simulation.

TASK #2

The channel model has been enhanced to include the ability to model a Nakagami-Rice fading characteristic. The Nakagami-Rice characteristic is similar to the Rayleigh fading characteristic with the addition of a non-fading quadrature term which is summed with the Rayleigh term at the receive antenna. The strength of the non-fading term is controllable by use of the user selectable 'multipath occurrence factor'. Digital programs were written and run which verified the hybrid simulation.

TASK #3

The following advanced modulation schemes were modeled and incorporated into the DRAMA simulation at the bandwidths given. These include 16 QAM, 8 PSK, and 49 QPR at 14 MHz bandwidth, 8 PSK, 64 QAM, and 49 QPR at 21 MHz bandwidth, and 64 QAM at 28 MHz bandwidth.

The rolloff of the baseband filters has been made a user-selectable option. The value of α can be set to .01, .25, .3, .5, .75, or .99 for any data rate, modulation scheme or bandwidth.

TASK #4

Remote terminal equipment necessary to control and analyze simulation runs has been supplied to DCEC, including a strip chart recorder. New, higher quality modems were used in the remote control of the hybrid simulation this year.

The remote user at DCEC has the option of viewing and setting all program options. The user can request power density spectrum plots of baseband, IF and RF. Signal constellation plots of the various modulation techniques are available to the user, as well as plots of the equalized and unequalized eye patterns.

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MONTHLY REPORTS

In addition to the tasks described above, monthly reports were written
and sent to the Defense Communications Agency as specified in the Statement
of Work.

3. ADVANCED MODULATION TECHNIQUES (MODTEQ) SIMULATION MODEL

This section describes the work performed in accordance with Task #3 of statement of work R220-85-011/Jan. 85. Task #3 requests the addition of bandwidth constraints and data rates to several advanced modulation techniques, namely PSK (8 level), QAM (16 & 64 level), and QPR (49 level). Accomplishment of these objectives was performed utilizing FY-85 funds. The following sections describe the specific techniques simulated under this contract followed by a discussion of the basic modules with which the sepecific techniques are realized.

3.1 PHASE SHIFT KEYING

The Simstar system is capable of simulating the eight-level PSK at a data rate of 45Mb/s with the capability of allowing user controlled selection of the Bandwidth Limiting Transmit Filter to either 14Mhz or 21Mhz. Figure 3-1 provides the block diagram for this modulation technique.

The Simstar host Gould 32/97 digital computer is used to generate and process data employed in this modulation technique. After generation of a random time-scaled 45Mb/s serial bit stream, a serial to 3 bit parallel conversion occurs resulting in a 15Msymbol/s stream. Three bit differential Grey encoder produces the analog input through a digital/analog converter.

The resulting eight level analog signal is multiplied by the angular factor $2\pi/8$ to determine phase angle (θ). Resolvers then compute the sine and cosine of the resulting phase angle for multipication of the IF carrier signals. The resultant expression, $\cos\theta\sin(\omega t)+\sin\theta\cos(\omega t)$ is then input to the bandwidth limiting transmit filter for user directed bandwidth constraint (14Mhz or 21Mhz).

The channel model used in the DRAMA radio model is set up modularly so that it is capable of being incorporated into the MODTEQ simulation. The channel model was designed and built for use with communication simulations and is described in Section 6.

Coherent demodulation is simulated with use of analog quarter square multipliers for incoming IF with the receiver IF carrier referenced oscillator. The resulting product is then passed to an integrate and dump circuit to recover the analog level representing the trigonometric product of the phase angle. The digital computer then interprets via analog/digital converter the 3 bit parallel symbol. By differentially decoding and performing a parallel to serial conversion, the transmitted 45Mb/s serial bit stream is then recovered.
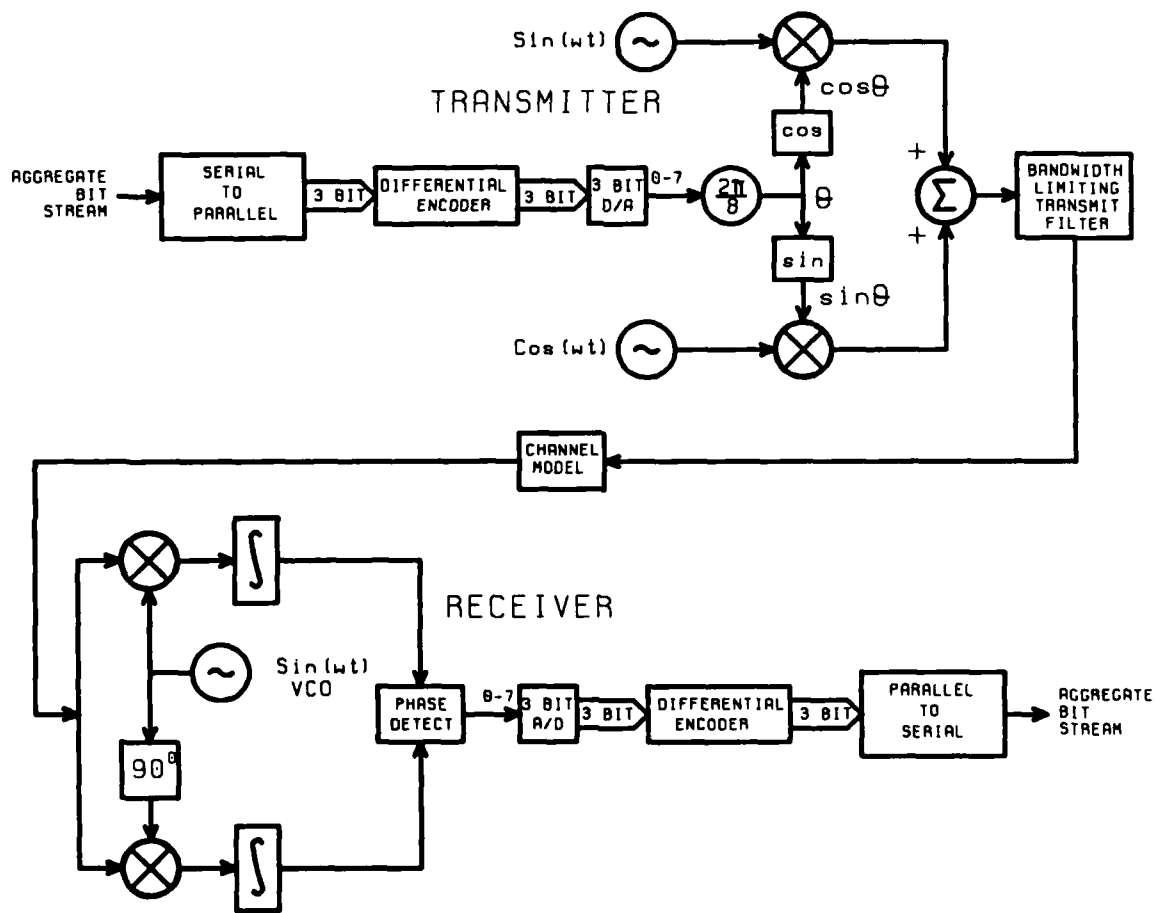
Figure 3-1 8 LEVEL PSK BLOCK DIAGRAM

3.2 QUADRATURE PARTIAL RESPONSE

Forty-nine level QPR at simulated data rates of 45Mb/s or 90Mb/s is implemented with the capability of allowing user controlled selection of the Bandwidth Limiting Transmit Filter to either 14Mhz or 21Mhz.   Figure 3-2 depicts the block diagram for this modulation technique.

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Using the digital computer, a random serial data bit stream is converted to two parallel 2 bit paths where differential decoding will take place. In one channel a half symbol delay will be provided for offsetting symbol streams. Digital/analog converters then apply the resultant 4 analog level to the baseband filters implemented on the AD-10 as described in Section 3.6 .
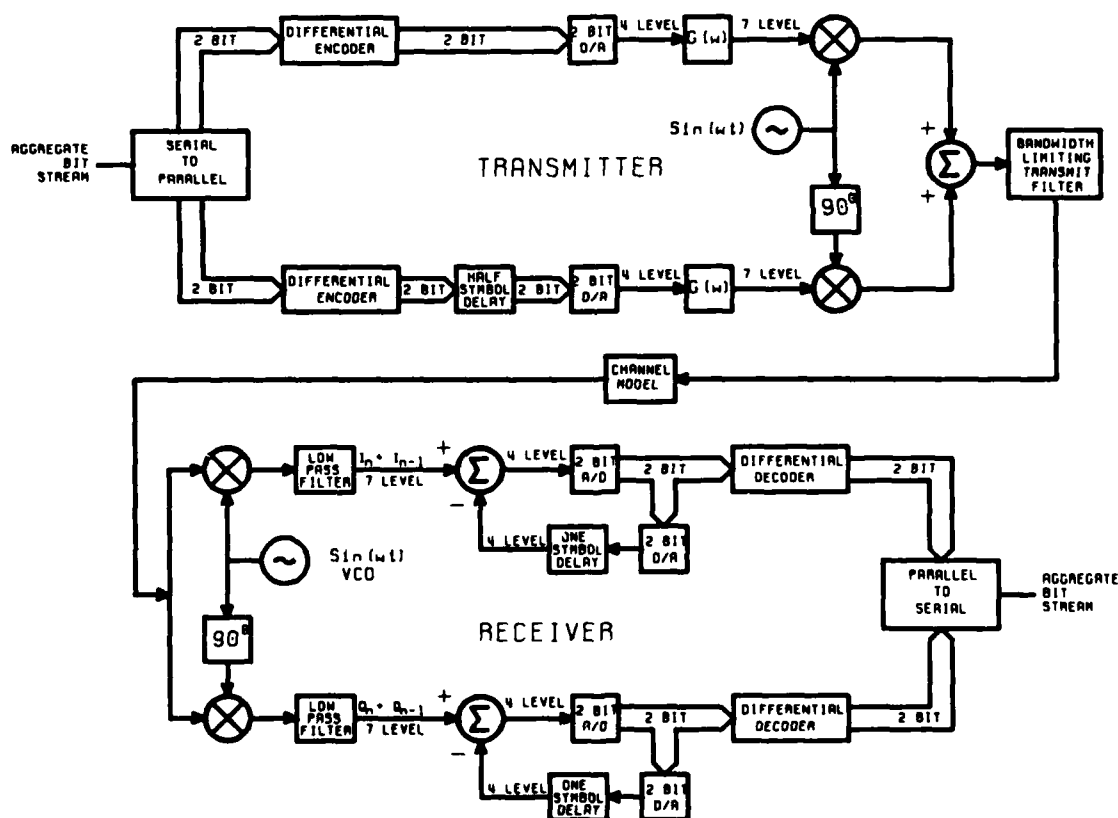
Figure 3-2   49 LEVEL QPR BLOCK DIAGRAM
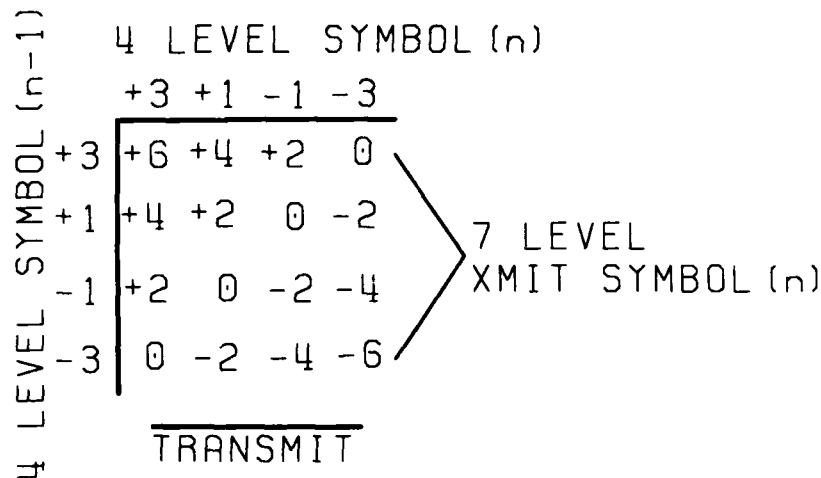
Figure 3-3 BASEBAND PULSE SHAPING: TRANSMITTER

The baseband filters are configured to provide a seven analog level output such that the amplitude of a given symbol is the summation of the prior input level and the present input level. See Figure 3-3 for clarity.

The parallel 7 level signals are then quadrature multiplexed to provide input to the Bandwith Limiting Transmit Filter which completes the transmit processing.

Again, the LOS channel model is user selectable and may be employed.

Coherent quadrature demultiplexing is employed in the receiver with low pass filters to extract the parallel 7 level symbols. The original 4 level signals are then recovered by subtraction of prior input signal (1 of 4) from present level (1 of 7). Figure 3-4 shows the method of recovering the original 4 levels. Note that levels indicated by (-) are invalid level transitions, since 4 states of 7 are the maximum transition change in the transmitter. Differential decoding then yields the original two parallel 2 bit streams which is then serialized to reproduce the original serial bit stream.

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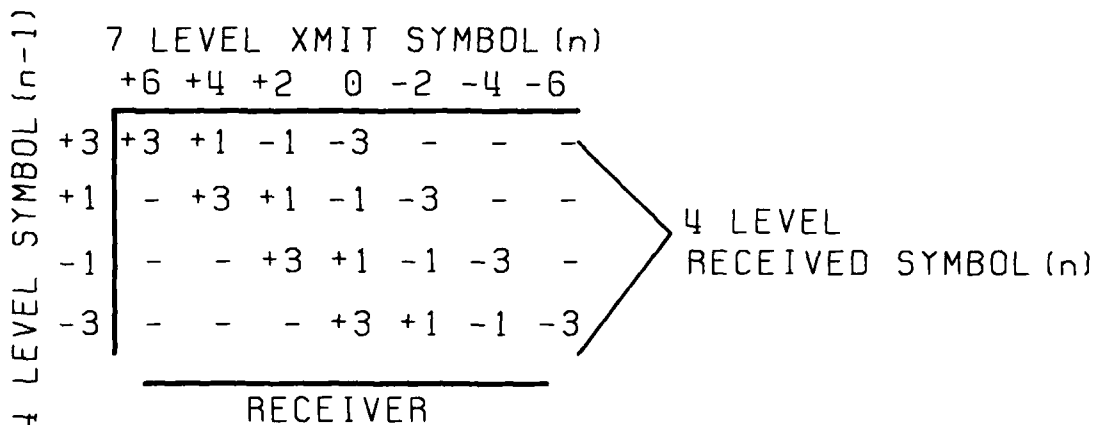
Figure 3-4   4 LEVEL RECOVERY: RECEIVER

3.3 QUADRATURE AMPLITUDE MODULATION

User controlled selection of the Bandwidth Limiting Transmit Filter is implemented for 16 or 64 level QAM at data rates of 45Mb/s (16 level), 90Mb/s (64 level), or 135Mb/s (64 level). Spectral band limiting is selectable for 14Mhz, 21 Mhz, and 28 Mhz. Figure 3-5 represents the block diagram for this modulation technique.

The digital computer produces a random serial bit data stream and performs serial to parallel conversion resulting in two parallel paths of 2 bit (16 level) or 3 bit (64 level) symbols. Differential encoding is then performed and resulting symbols are input to the analog section of the simulation via digital/analog converters providing 4 or 8 level analog signals to the baseband filters.

The baseband filters in this technique are configured to eliminate inter-symbol interference. These are described in Section 3.6 . Baseband outputs then drive the quadrature multiplexer providing transmit IF signal to the Bandwidth Limiting Filter.

Again, the LOS channel model is user selectable and may be employed.

Coherent demodulation is simulated by analog multiplication of the incoming IF and the receiver IF carrier referenced oscillator coupled to a low pass filter. Analog/digital conversion extracts the 2 bit (16 level) or 3 bit (64 level) symbol streams from the analog level. These two parallel

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streams are differentially decoded and serialized to reproduce the original data input stream.
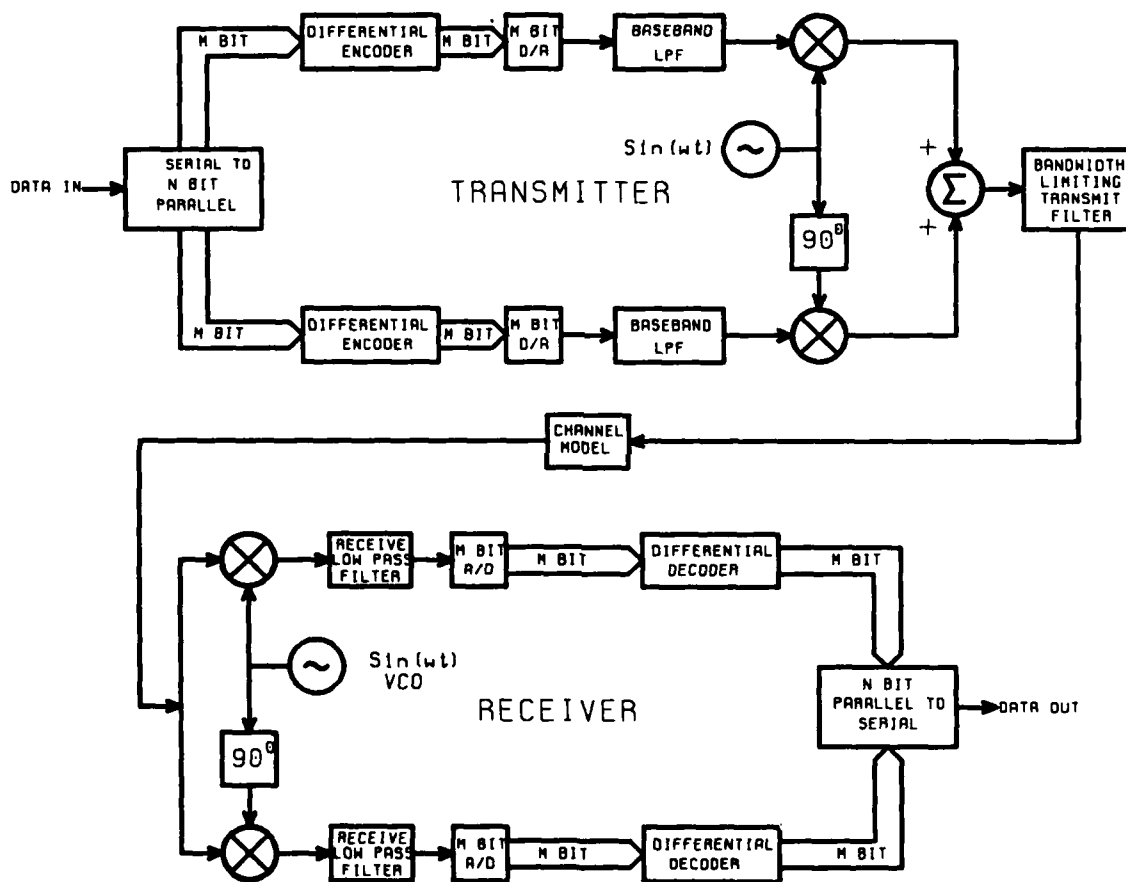
Figure 3-5   16 and 64 LEVEL QAM

3.4 MODTEQ: BASIC MODULES

Figure 3-6 depicts the basic modules in block form utilized in the MODTEQ simulation.   This diagram and the following descriptions in conjunction with the programs found in Appendix A provide a thorough description of the simulation.

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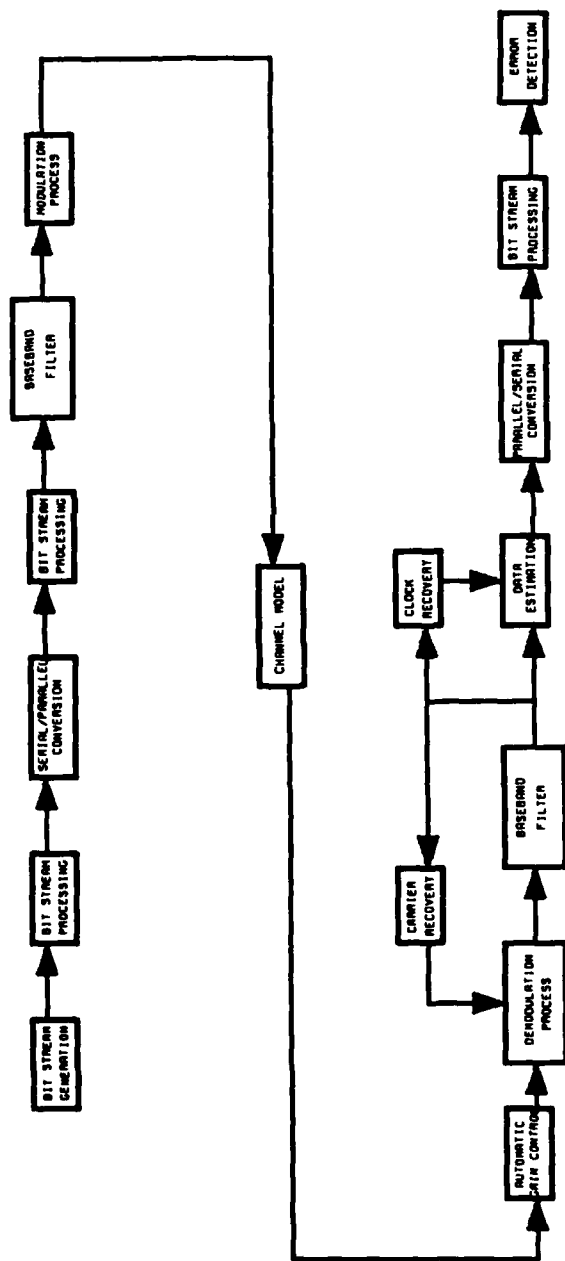
Figure 3-6 MODULATION TECHNIQUES BLOCK DIAGRAM

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3.5 DIFFERENTIAL ENCODING/DECODING

It is possible that the transmitter carrier and the receiver carrier will lock up 180 degrees out of phase. All received bits will be inverted when demodulated if this occurs. For this reason, the message is differentially encoded before modulation. When decoding a differentially encoded message, changes in sign between consecutive bits convey the message, not the signs of the bits themselves; therefore, it doesn't matter if the signs are inverted. In general the encoding follows the equation

$$d_k = d_{k-1} \; O \; b_k$$

The differential encoding sequence, d_k, is produced from an input sequence, b_k, starting with an arbitrary first d_k, say 1, and thereafter d_k toggles whenever there is a difference between b_k and d_{k-1}.

The encoded bit stream is decoded at the receiver by checks to see if the phase angles of the received carrier during two successive bit intervals are the same or different. With an initial phase angle of 0 for the reference bit, the receiver output is 0 at the end of a signaling interval if the carrier phase was the same as during the previous interval. If the phase angles are different, then the receiver output is 1.

3.6 TRANSMIT BASEBAND FILTERS

Section b of Task 3 of the statement of work outlined the requirement to be able to adjust the baseband filter rolloff, or 'alpha', of the transmit baseband
filters for each of the following modulation types:

o

o 16 QAM @ 45 Mb./s & channel bandwidth of 14 MHz

o   8 PSK @ 45 Mb./s & channel bandwidth of 21 MHz

o   8 PSK @ 45 Mb./s & channel bandwidth of 14 MHz

o 49 QPR @ 45 Mb./s & channel bandwidth of 14 MHz

o 64 QAM @ 90 Mb./s & channel bandwidth of 21 MHz

o 49 QPR @ 45 Mb./s & channel bandwidth of 21 MHz

o 64 QAM @ 135 Mb./s & channel bandwidth of 28 MHz

In January of 1985, a meeting between Martin Marietta engineers and Defense Communication Engineering Center engineers was held at the Reston, Virginia DCEC location. Among the topics discussed was the requirement to allow adjustment of the rolloff factor for QPR and PSK systems. It was brought out at that meeting that alpha was not adjustable for QPR and 8 PSK systems due to the fact that QPR and PSK systems do not use raised cosine filters and that the requirement to provide that capability would be waived for those particular systems. Additionally, the adjustment of alpha and the channel bandwidth limiting IF filter should be done hand-in-hand, since for a given alpha in a given system there is an optimal channel bandwidth. Still, the requirement for the adjustable alpha for QAM systems existed and the following is a description of the implementation of that capability.

A raised cosine filter is a particular type of low-pass filter used as a baseband filter. This filter eliminates intersymbol interference. There is a particular parameter called 'alpha', rolloff factor, or excess bandwidth, which shapes the impulse response, and therefore the frequency response of the filter. As alpha is increased from its minimum value of zero to its maximum value of one, the extent of the *Fourier transform of the impulse* response grows from half the symbol rate at alpha=0, to the full symbol rate at alpha=1. This is depicted in Figure 3-7. Naturally there is an associated change in the impulse response. At alpha=0, the filter requires minimum bandwidth. The price to pay for the minimum bandwidth advantage is the fact that there is a maximum of overshoot and ringing in the impulse response. This increases the bit error rate due to clock jitter in the receiver. This ringing also has the disadvantage of using up power at IF and RF in order to exist and causes extensive IF envelope modulation which is generally considered undesirable. Another problem with alpha=0 is the necessity of having a 'brick-wall' filter. Close approximations are acceptable but difficult to implement reliably.

At the other end of the range, where alpha=1.0, the filter is more easily implemented, and there is little ringing to create the problems associated with a small value of alpha. The disadvantage of a large alpha is the fact that the channel bandwidth required to accomodate the modulated baseband signal is proportional to 1+alpha. Typically, a compromise of alpha in the range of 0.2 to 0.4 is considered optimal. The impulse responses of the filter for various values of alpha are provided in Figure 3-8.
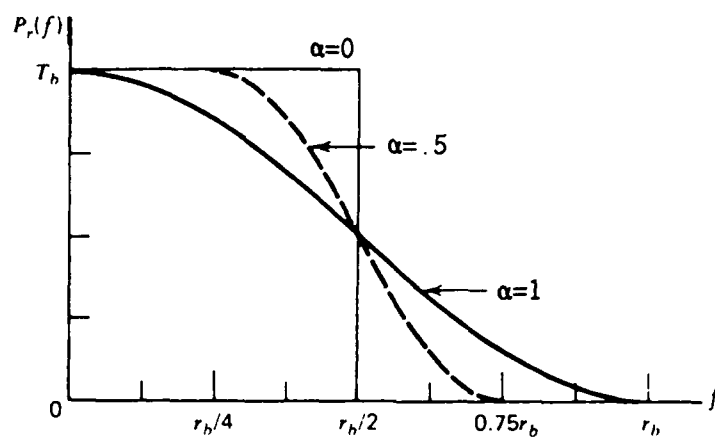
Figure 3-7   RAISED COSINE FREQUENCY RESPONSES
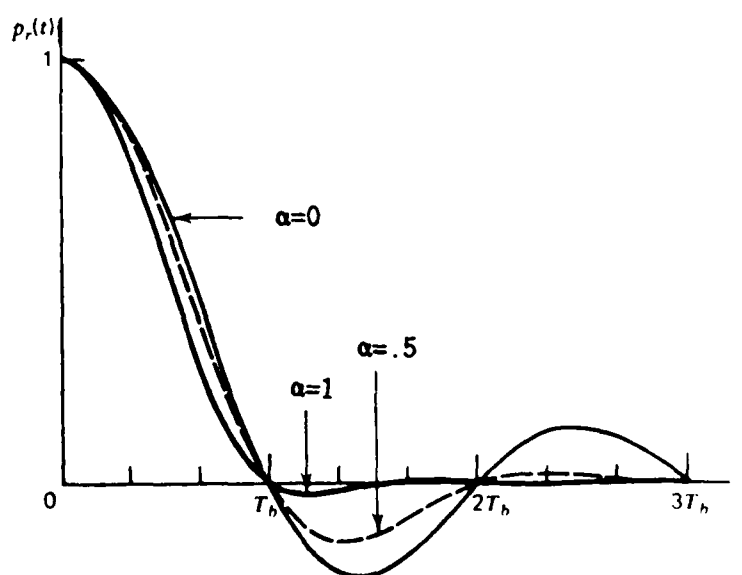
Figure 3-8   RAISED COSINE IMPULSE RESPONSES

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The form of the frequency response is as follows:

$$H(f) = \begin{cases} 1 & |f| \le (1-\alpha)/(2T) \\ \cos^2\{ \ (\pi|f|t)/(2\alpha)-\pi(1-\alpha)/(4\alpha) \ \} & (1-\alpha)/(2T) \le |f| \le (1+\alpha)/(2T) \\ 0 & \text{otherwise} \end{cases}$$

The form of the impulse response is as follows:

$$h(t) = \sin(\pi t/T)\cos(\alpha \pi t/T) \ / \ \{ \ (\pi t/T)[1 - (2\alpha t/T)^2] \ \}$$

Inspection of Figure 3-8 and the equation for the impulse response shows that the impulse response crosses through zero at multiples of T, the symbol period for any value of alpha. This is what produces the zero intersymbol interference. An extensive period of time was devoted to producing analog filters which would provide the exacting requirements, including the zero crossings. The appoach taken was to use numerical techniques to find the poles of an appropriate transfer function to yield a frequency response that matches that stated above. Although this was done successfully, the time response did not match closely enough to qualify as a reasonable approximation. Another approach was then pursued.

The second method provided an excellent solution. The entire problem was solved in the time domain. This was done by programming a separate digital processor, the Applied Dynamics International AD-10 as a pair of transversal filters, one for the I channel, and one for the Q channel. Textbook perfect impulse responses were obtained by this method.

An impulse response is stored in the AD-10 and a time history of the filter input is convolved during the real time run. The processor combines the effects of the present symbol and 17 previous symbols to eliminate significant impulse response truncation. The worst case impulse is damped a negligible amount in the 18 symbol time history stored in the processor. The user is capable of requesting alphas of 0.01, 0.25, 0.30, 0.50, 0.75, and 0.99 for use in the radio model.

For QPR, the the impulse response is such to utilize large amounts of intersymbol interference in a very controlled manner. This eliminates the following problems associated with small values of alpha in a QAM system:

o Complex & sensitive filters

o Clock jitter problems

o Excessive ringing

QPR also uses as little channel bandwidth as a QAM system with an alpha equal to zero. The price to be paid for these advantages is a 3 dB Eb/N0 loss in performance. Figure 3-9 depicts the Fourier transform of the impulse response.   Note that the frequency domain representation is limited to +/- half the symbol rate as is the QAM system of Figure 3-7 for alpha=0. Figure 3-10 shows the impulse response. Note that the width of the main lobe of the response is such that it covers two adjacent symbols. This causes the large amounts of intersymbol interference.

The form of the frequency response for partial response is as follows:

$$H(f) = \begin{cases} \cos(\pi|f|T) & |f| \leq 1/(2T) \\ \\ 0 & \text{otherwise} \end{cases}$$

The form of the impulse response for partial response is as follows:

$$h(t) = 4\cos(\pi t/T) \, / \, \{ \, \pi[1 - (2t/T)^2] \, \}$$

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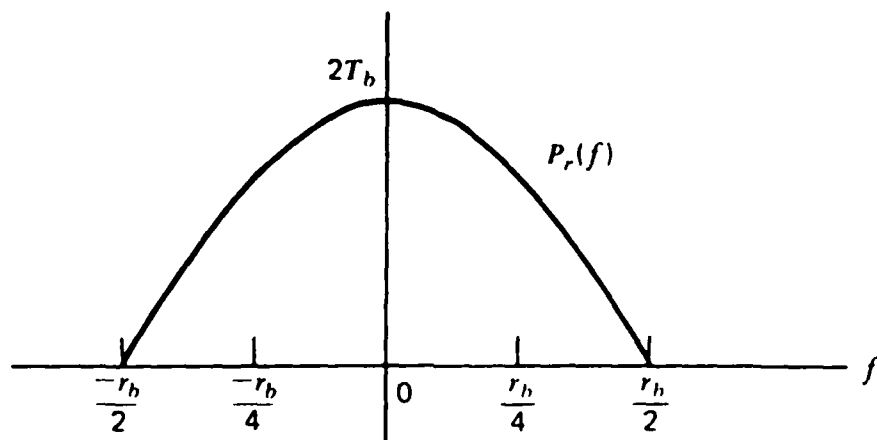
Figure 3-9   PARTIAL RESPONSE FREQUENCY RESPONSE
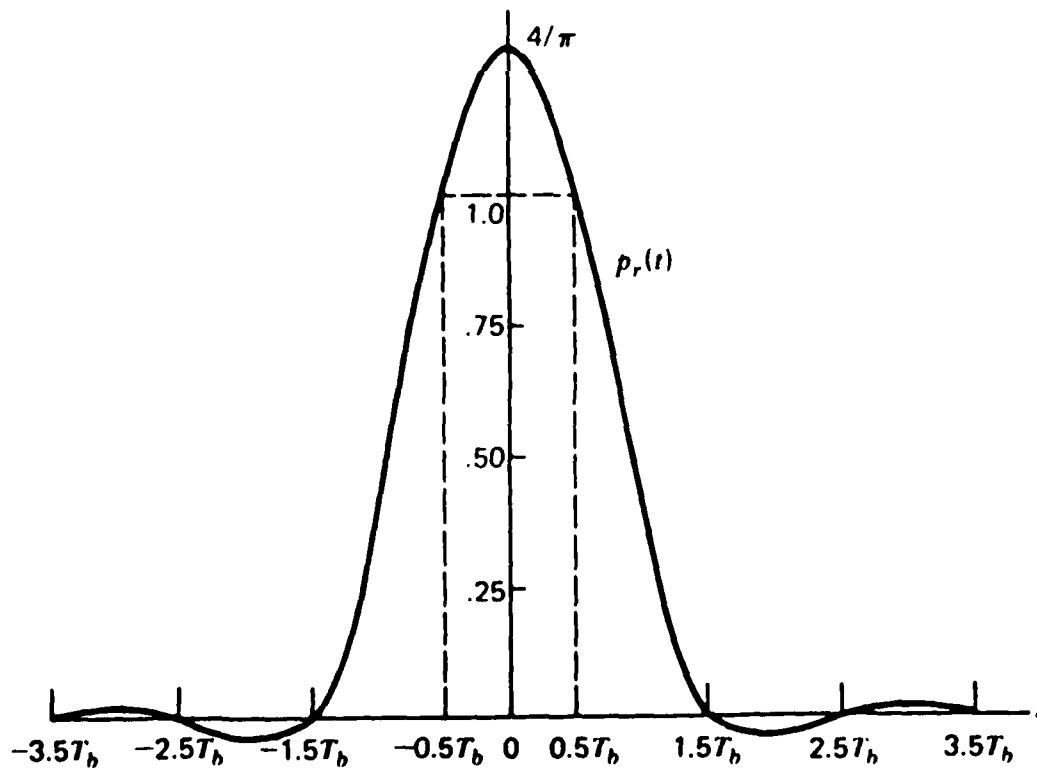
Figure 3-10   PARTIAL RESPONSE IMPULSE RESPONSE

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3.7 IF FILTERS

The IF filter model is a 6-pole bandpass filter. The IF filter is programmed to model characteristics of Butterworth, Bessel and Chebychev bandpass filters employing normalized lowpass frequency transformations. Bandwidth, center frequency and ripple factor are also programmed parameters and may be changed with user software. To find the Chebyschev approximation for a bandpass filter the normalized lowpass poles are calculated by

$$s_k = \sigma_k +/- j\omega_k \quad k=0,1,2,3,\ldots,2n-1$$

$$\sigma_k = +/- \sin\left[\,\pi(1+2k)/(2n)\,\right]\{\,\sinh[\,\sinh^{-1}(1/\epsilon)/n\,]\,\}$$

$$\omega_k = \cos\left[\,\pi(1+2k)/(2n)\,\right]\{\,\cosh[\,\sinh^{-1}(1/\epsilon)/n\,]\,\}$$

The lowpass function is then transformed to a bandpass function. The frequency transformation that accomplishes this is

$$S = (\,s^2 + \omega_0^2\,)/(Bs)$$

where

$$B = \omega_2 - \omega_1 \quad \text{is the bandwidth}$$

$$\omega_0 = (\omega_1\omega_2)^{1/2} \quad \text{is the center of the passband}$$
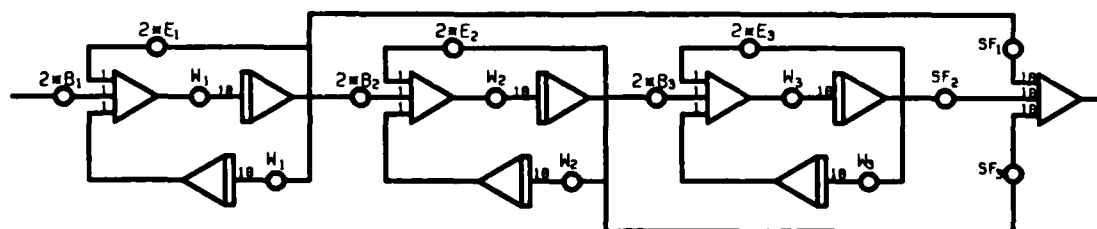
Figure 3-11 BANDWIDTH LIMITING FILTER SIMULATION

This filter model is used for PSK, QAM, and QPR radio models.

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3.8 AUTOMATIC GAIN CONTROL

The automatic gain control circuit full wave rectifies the output of the IF filter. A peak rider then detects the average amplitude, which is then subtracted from the reference amplitude. This difference or error is cubed and integrated to drive multipliers at the input of the IF filter to achieve the reference amplitude. Figure 3-12 is a block diagram of the AGC configuration used for all of the MODTEQ simulations. This AGC circuit can achieve gains of 42 dB. This same AGC design services the QPR and QAM simulations as well as PSK.
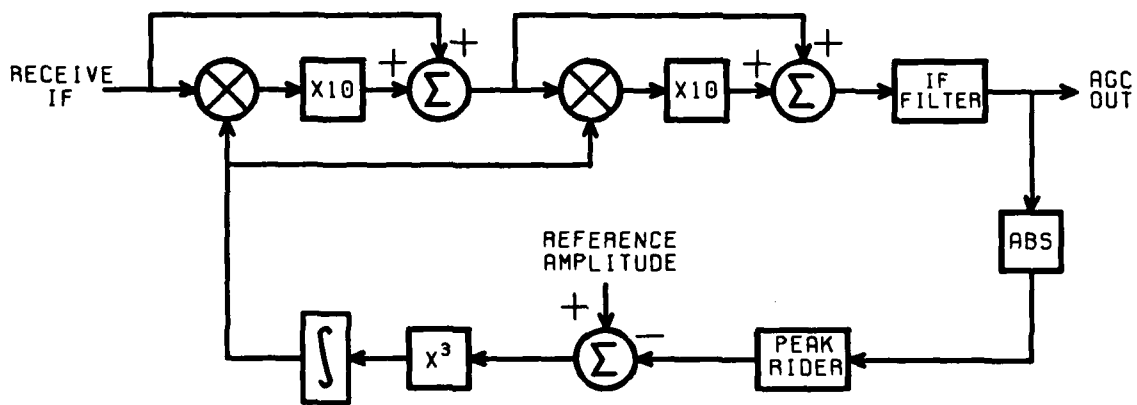
Figure 3-12   AUTOMATIC GAIN CONTROL

3.9 CARRIER RECOVERY

The receiver carrier of the simulated radio is phase locked to the transmitter carrier using a modified Costas loop. This method of demodulation extracts the two signal streams by multiplying the received IF signal by the in-phase and quadrature components of the phase locked reference oscillator and then lowpass filtering to remove the double-frequency components. The lowpass filters are 4th-order Chebyshev type.

The in-phase and quadrature basebands are then input to two quantizers which are used as data estimators. The quantizers are described in a separate section of this report.

The phase locked_ loop uses a cross correlation between the quadrature symbol streams' low-pass filter outputs and hard decision estimates from the quantizers to generate a phase error signal. A difference of the resulting cross correlations is filtered by the phase locked loop filter and input to the reference VCO to phase lock it to the modulated carrier. The carrier recovery circuit is shown is shown in Figure 3-13.

The phase locked loop (PLL) filter is wideband during acquisition of lock and is then switched to narrowband when lock occurs. The phase lock loop filter circuit is shown in Figure 3-14.
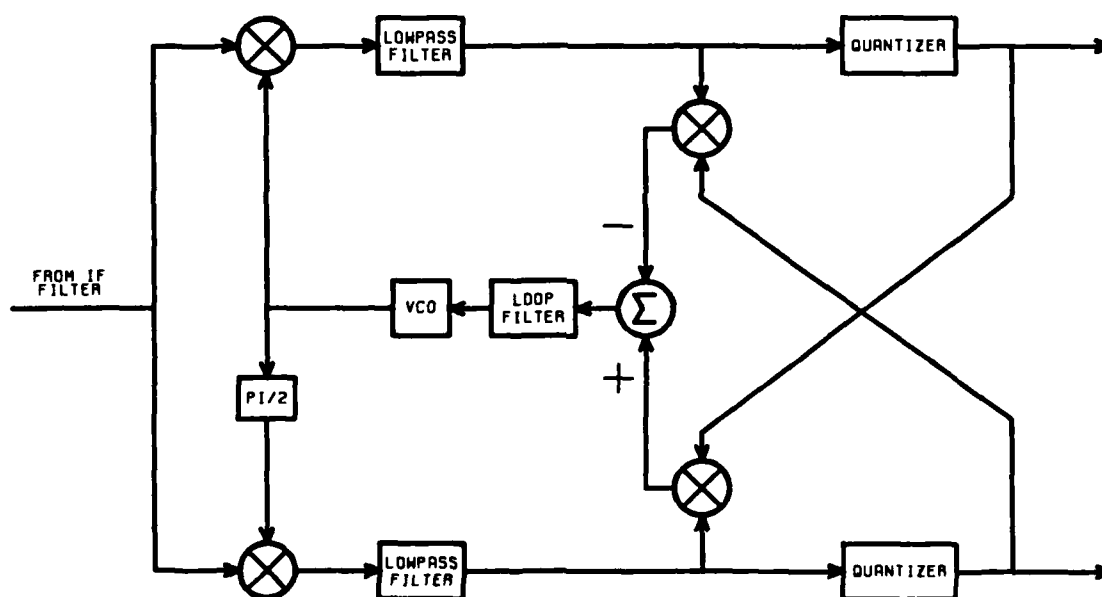
Figure 3-13   CARRIER RECOVERY CIRCUIT

3.10 CLOCK RECOVERY

A triangle wave VCO is used to obtain clock recovery. The control voltage is dependent upon the product of the missed distance between the baseband and the quantized level of the baseband and the slope of the baseband at sample time. The slope of the baseband is taken from the first derivative of the output of the 4th-order LPF which produces the baseband.

A quantizer was developed to determine the quantized level of the baseband. The quantizer can be used for both QAM and QPR modulation

techniques with any number of levels. The user must set the number of bits per symbol (BITPSM) and the offset (OSET) to obtain the desired quantization levels. For an even number of levels an offset of 0.5 is desired, and for an odd number of levels an offset of 0.0 is desired.

The example in Figure 3-15 shows the miss distance and slope when the phase of the clock oscillator is lagging the baseband signal. In this case, the miss distance is positive and the slope of the baseband is negative. Thus, the product of the two is negative. This product controls the VCO by decreasing the amplitude of the triangle wave and consequently increasing the frequency of the clock.

In the case where the clock oscillator phase leads the baseband signal, the sample time occurs too soon. This will yield a positive product which will increase the amplitude of the triangle wave and therefore decrease the frequency of the clock.
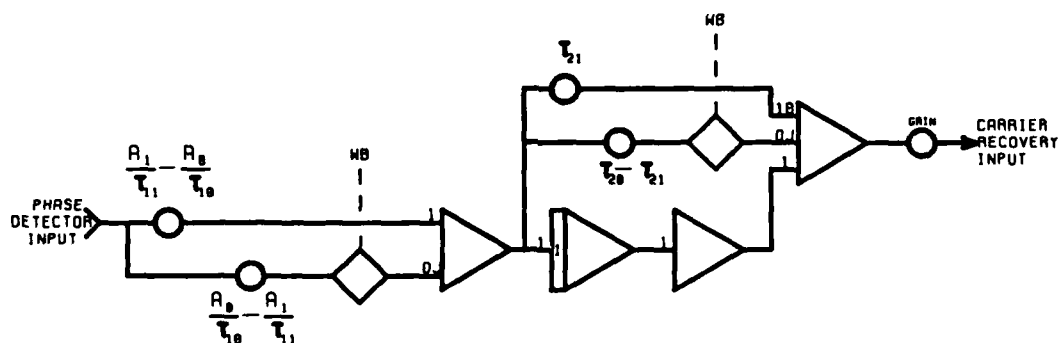
Figure 3-14 PHASE LOCK LOOP FILTER
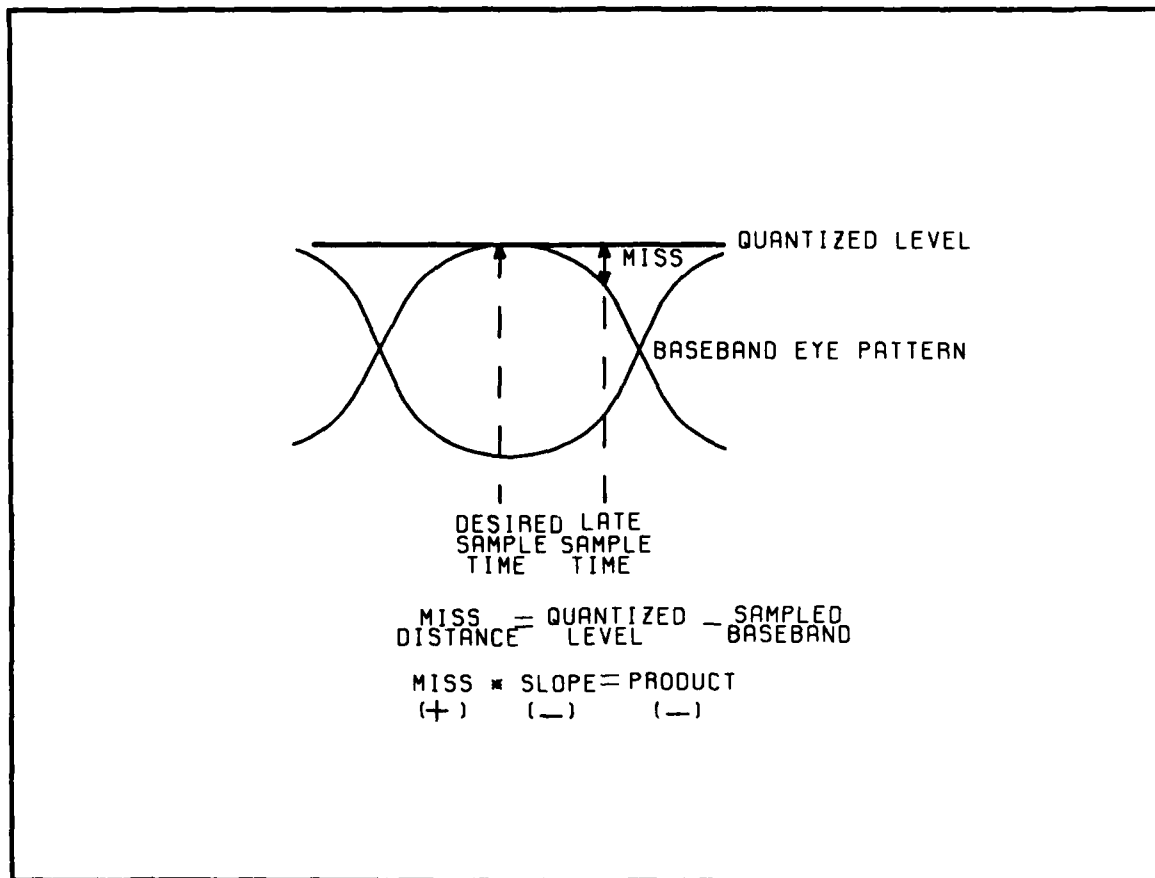
Figure 3-15   VCO CONTROL EXAMPLE

The layout for the clock recovery circuit is shown in Figure 3-16. An electronic switch controlled by the VCO toggles between the I and Q channels. The output of this switch is fed to a track/store integrator which is always in the track mode except for a brief sample time. This output is then drives a PLL filter which directly controls the VCO frequency.
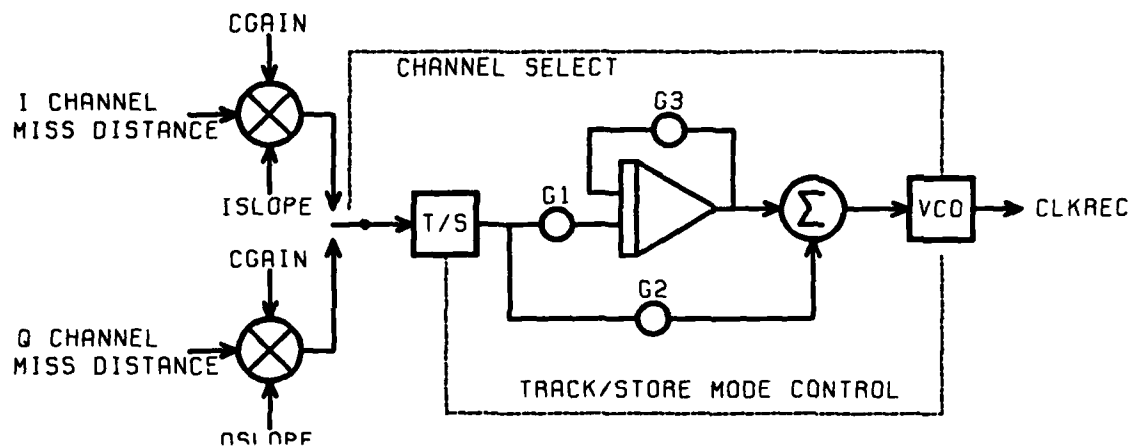
Figure 3-16 CLOCK RECOVERY CIRCUIT

REFERENCES

Bellamy, J. Digital Telephony. New York: John Wiley and Sons, Inc., 1982.

Shanmugam, K.S. Digital and Analog Communication Systems. New York:
John Wiley and Sons, Inc., 1979.

4. AN/FRC-170(V) DUAL DIVERSITY SIMULATION MODEL

This section describes the modeling and simulation of the AN/FRC-170(V) dual diversity radio. The major subsystems of this line-of-sight (LOS) transmission system model are the transmission section, dual receivers, IF equalizer and baseband equalizer. Both quadrature partial response (QPR) and quadrature phase shift keyed (QPSK) transmission techniques for Level II and I, respectively, have been incorporated into the system simulation.

The hybrid computer model of the DRAMA radio includes the unique characteristics of the AN/FRC-170(V) radio. These include Level I quadrature phase shift keyed (QPSK) performance rates to 13.065 megabits per second (MBS) and Level II quadrature partial response (QPR) performance at rates to 26.112 MBS. Other features are the switching of baseband filters for QPR and QPSK transmission, two and three level detection of the received baseband, and the signal processing required for measurement, signal quality, and diversity switch circuits peripheral to the radio. Figure 4-1 is an overall layout of the system.

The hybrid computer simulation of the DRAMA radio provides a programmable scale model which may be configured and changed by the simulation user to evaluate performance and design for anticipated deployments. This model has been implemented by frequency scaling models of the prototype modem to permit simulation on the hybrid computer and use of special purpose hybrid delay line hardware. Even with this time scaling, the hybrid simulation is 100 times faster and more efficient than equivalent digital simulation methods. The current scale factor for the DRAMA radio simulation is 26,112, which results in simulation IF, data rate, and baseband baud rate frequencies of 2,681 Hz, 1,000 Hz, and 500 Hz, respectively.

Major simulation modules for the DRAMA QPR/QPSK radio are bit stream generation and processing, QPR/QPSK modulation, transmitter signal processing, dual diversity receivers and data regeneration. Design parameters for filters, data rates, phase lock loops (PLL), nonlinear devices, and automatic gain control (AGC) circuits have been accounted for in the simulation model. Validation of the DRAMA radio model and simulation under a previous contract, was based on actual bit error measurements taken from the DRAMA radio prototype. Figure 4-2 is a plot of this data.

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Figure 4-1 OVERALL DRAMA SYSTEM LAYOUT

QPR OR QPSK RECEIVERS

IF COHERENT COMBINER → IF FILTER AND AGC A → f_{F_A} → MODIFIED COSTAS LOOP A → BASEBAND EQUALIZER → TWO AND THREE LEVEL DETECTOR A → DATA RECOVERY A → DIFFERENTIAL DECODER → PARALLEL TO SERIAL CONVERTER A → x_{AS} → DESCRAMBLER A → TDM DEMUX

BIT ERROR DETECTION → ERRORS

ADAPTIVE THRESHOLD A

CLK A/2

CLOCK RECOVERY → CLK A

PERFORMANCE MONITOR MODULE
• AGC
OTR
PSUEDO ERROR

DIVERSITY SWITCH ALGORITHM

DIVERSITY SWITCH → RECEIVED DATA

DIGITAL CLOCK AVERAGING

CLK B

CLOCK RECOVERY B

CLK B/2

ADAPTIVE THRESHOLD B

IF COHERENT COMBINER → IF FILTER AND AGC B → IF_B → MODIFIED COSTAS LOOP B → BASEBAND EQUALIZER → TWO AND THREE LEVEL DETECTOR B → DATA RECOVERY B → DIFFERENTIAL DECODER B → PARALLEL TO SERIAL CONVERTED B → x_{BS} → DESCRAMBLER B → TDM DEMUX

* - OPTIONAL MODULE
v - VARIABLE MODULE

25
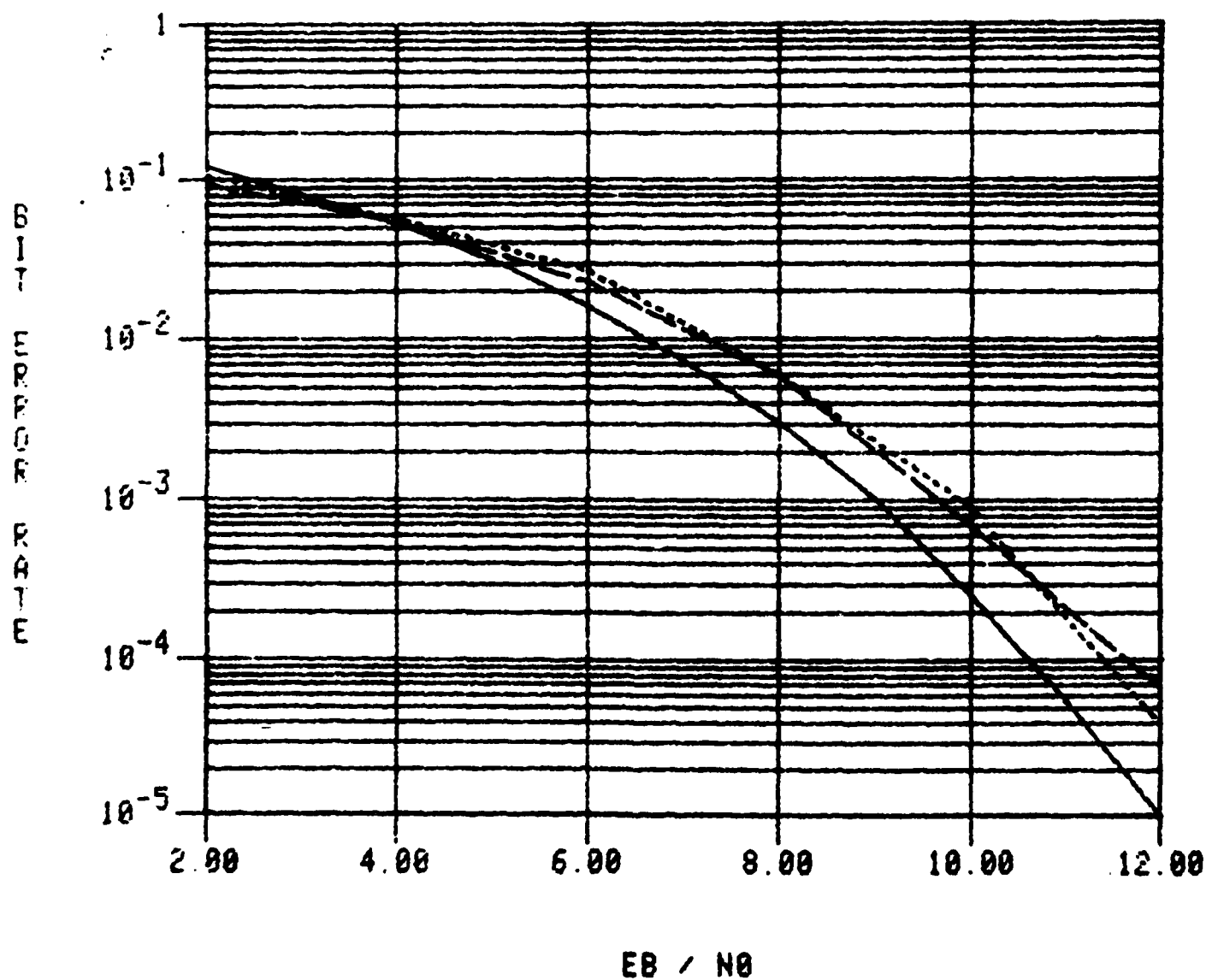
Figure 4-2 QPR BER vs. EB/N0

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4.1 BIT STREAM GENERATION AND PROCESSING

The bit stream generation for the DRAMA radio is the same for both QPR and QPSK. This module includes a random data generator, an optional 20-bit self-synchronizing scrambler, serial-to-parallel converter, and differential encoder. An optional TDM framing pattern is also available and is described in Section 5.3. A functional flow diagram for these circuits is shown in Figure 4-3. The data generator provides the pseudo-random data input which would be present at the multiplexer output ports. A self-synchronizing scrambler with 20 stages was modeled to ensure a random modulating bit stream. This circuit, which eliminates long series of ones or zeros from occurring in the modulating bit stream, has been provided as an option and may be bypassed. The randomness guaranteed by implementing the scrambler results in a better spectral component of the bit rate clock at the receiver clock recovery circuit as a result of additional data transitions.

A model of the scrambler used in the DRAMA radio was obtained by modulo 2 summing the serial data stream with the modulo 2 sum of bits 17 and 20 of a 20-stage shift register. The scrambled or unscrambled data were input to the serial-to-parallel converter. The serial-to-parallel converter was mechanized by retiming the scrambled output with the symbol clock (one-half the data rate). Symbol timing is used to clock the I and Q data out with a one-half symbol delay with respect to one another. This improves resolution of the two-phase ambiguity states at the receivers. Each of these parallel bit streams is input to differential encoders which resolve any polarity inversion at the demodulator. These encoders are modeled as a modulo 2 sum, (exclusive "OR"), and delay flip-flop type encoders. These circuits do a logical multiply of the feedback and data. Outputs from the two encoders provide the inputs to the modulation circuit.

Except for data generation which consists of a broadband noise source and analog sampler (track/store integrator), the message data input module is simulated using the parallel logic capability of the analog computer. Time division multiplexing framing patterns are supplied by the digital computer at the proper time and are multiplexed into the data stream. Modulo 2 sums and differential encoders were programmed using a combination of gates and flip/flop delays. The scrambler uses five 4-stage shift registers in series to provide the 20-bit delay. Serial-to-parallel conversion was simulated by using flip/flops enabled by inverted symbol clocks to provide a one-half symbol delay between one symbol bit stream and the other.

27
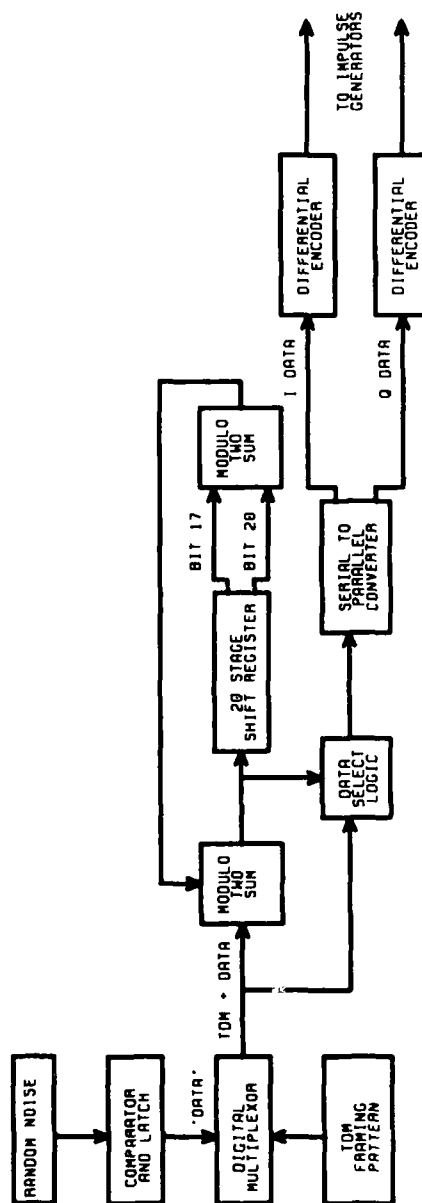
Figure 4-3 DATA GENERATION AND PROCESSING

4.2 QPR/QPSK MODULATOR

The simulated AN/FRC-170(V) radio modulator section includes impulse generators for QPR transmission, digital to analog switches, transmit baseband filters, in phase and quadrature multipliers, and a crystal controlled reference oscillator. Input to the modulator module is from the I and Q differential encoders. Figure 4-4 is a functional flow block diagram of the major circuits for the modulator simulation.
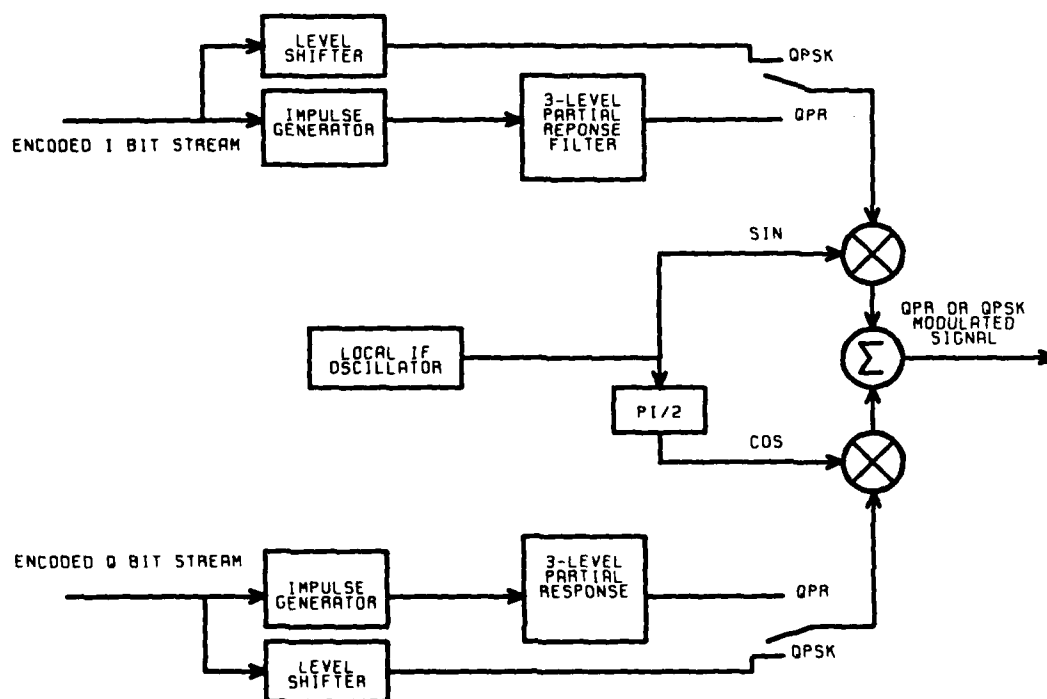
Figure 4-4 QPR/QPSK MODULATOR

The simulation allows both QPSK and QPR modulation techniques. If QPSK modulation is selected, a path is provided directly from the I and Q nonreturn to zero (NRZ) data to digital-to-analog switches which generates +1 and -1 logic. The +1 and -1 logic for the I and Q channels is multiplied by the sine and cosine outputs of the reference oscillator to generate the modulated I and Q signals. The I and Q modulated signals are then summed to provide the QPSK signal.

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If QPR is selected, the I and Q NRZ signals are input to impulse generators. The impulse generators control the digital to analog switches that drive the partial response filters. The impulse generators were mechanized using monostable flip-flops (one shots). These devices have an adjustable pulse width which was set to provide the desired impulse response from the partial response filters. The outputs of the partial response filters were multiplied by the sine and cosine outputs of the reference oscillator to generate the modulated I and Q signals. The I and Q modulated signals are then summed to provide the QPR IF signal. The crystal controlled reference oscillator for this modulator section was programmed using two analog integrators with feedback to stabilize the amplitude and a crystal controlled digital clock to maintain a fixed frequency.

The modulator circuits were programmed using both logical and analog computer techniques. Programs developed for the modulation function and all other functions of the DRAMA radio simulation were under control of the digital computer. This facilitates parameter and configuration changes, setup procedures, and data acquisition.

4.3 BASEBAND PARTIAL RESPONSE

The baseband filters implemented in the simulation are 7th order transmit and 5th order receive elliptical filters. The filters have been modeled to match the theoretical responses of the AN/FRC-170(V) filters. Both transmit and receive filters have been mechanized on the analog computers using standard analog implementation of bi-quadratic sections.

More efficient use of equipment in other areas of the simulation has allowed the 5th order receive and 7th order transmit filters to be included in the simulation as a permanent addition.

4.4 TRANSMITTER SIGNAL PROCESSING

A typical transmission section was modeled for the AN/FRC-170(V) radio. This configuration includes two transmitter bandpass filters for spectral limiting and a TWT power amplifier. All of these devices are modeled on the analog computer and can be configured by the simulation user.

Optional spectral control bandpass filters and an optional nonlinear amplifier were simulated for the transmission module. These bandpass filters were programmed to permit the selection of either Butterworth, Bessel, or Chebychev characteristics for two, four, or six poles. A stagger-tuned simulation approach was taken, where the parameters for each stage were calculated and set by the digital computer, based on parameter inputs by the user for center frequency, ripple and bandwidth. The digital computer then calculates and sets the parameters of each stagger-tuned section to produce the desired overall frequency response of the filter.

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Referring to Figure 4-5 the filter parameters B, E, and W of
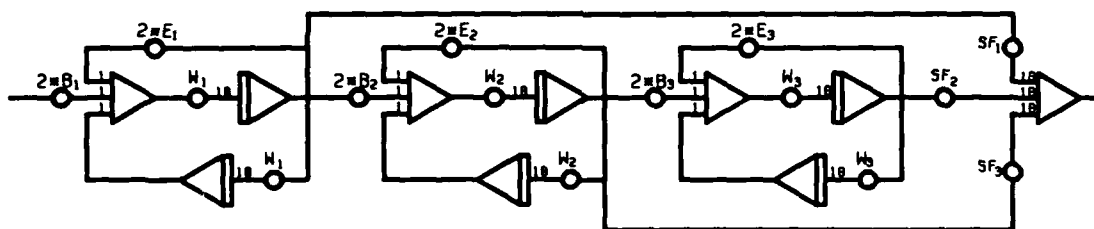
Figure 4-5   BANDPASS FILTER SIMULATION

each stage represent the gain bandwidth product, bandwidth, and center frequency, respectively.   SF1, SF2, and SF3 are the scale factors that adjust the overall gain of the filter to ensure unity gain and select the order of the filter.

The nonlinear device subsystem simulates the AM/AM and AM/PM characteristics of the AN/FRC-170(V) radio TWT.*   The TWT simulation is shown in Figure 4-6. Both the AM/AM and AM/PM characteristics of the DRAMA TWT are generated by the multi-function table processor (MFTP).

The MFTP is a high speed special purpose digital device designed to perform the operations of table lookup and linear interpolation in a manner to generate functions of one to four variables from preloaded data tables.

The modulated carrier is input to an envelope detector, which determines the time-varying amplitude of the carrier by diode detecting the signal magnitude and filtering out the carrier frequency.

This amplitude output drives the two functions in the MFTP which are loaded with the AM/AM and AM/PM characteristics of the nonlinear device. The output of the AM/PM function determines the time constants for an analog computer programmed phase shifter that shifts the modulated carrier by the corresponding gain. Graphs of AM/AM and AM/PM characteristics for the TWT are shown in Figures 4-7 and 4-8.

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*   Thomas, C. M., Alexander, J. E., and Rahnebert, E.W., "A New Generation of Digital Microwave Radios for U.S. Military Telephone Networks," IEEE Transactions on Communications, Vol. Com-27, No. 12, December 1979.
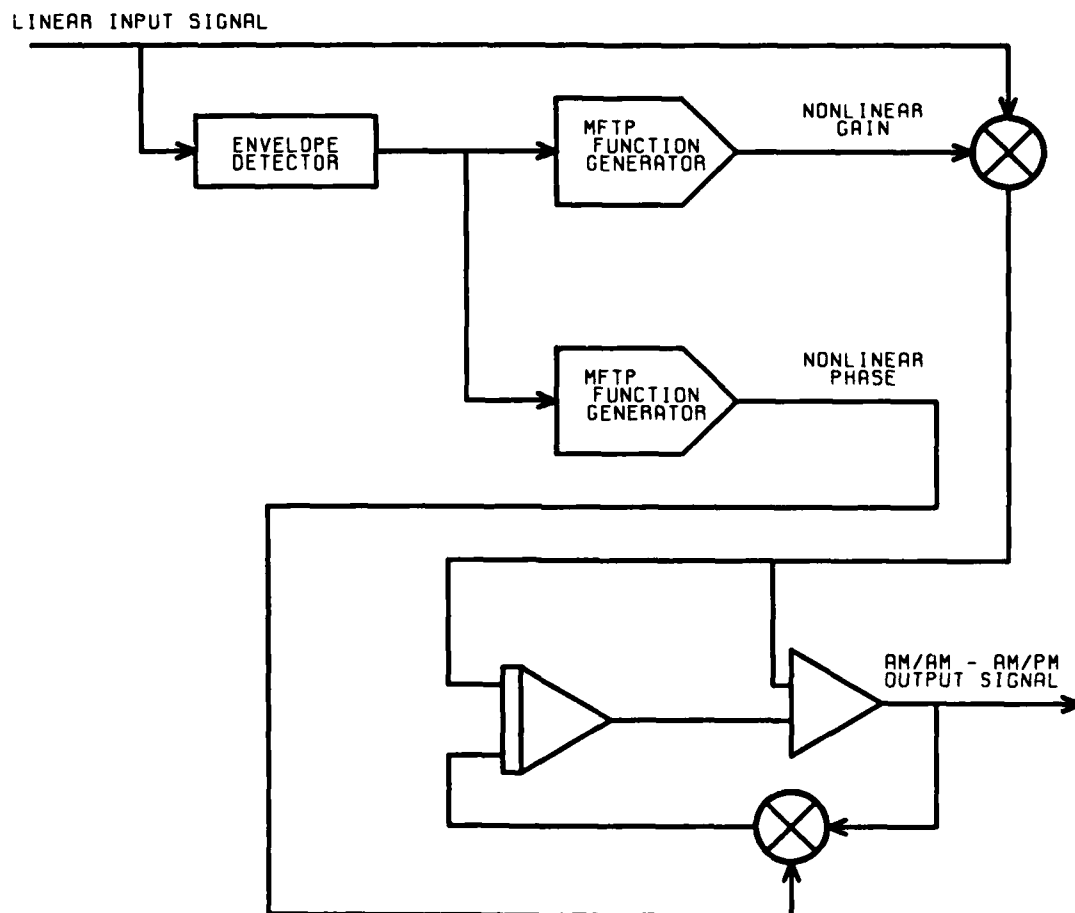
Figure 4-6 NON-LINEAR DEVICE IMPLEMENTATION

The characteristics of the TWT model are stored in a data file which is loaded into the MFTP. A separate data file will be generated for each TWT model allowing the simulation user to choose which model will be implemented.
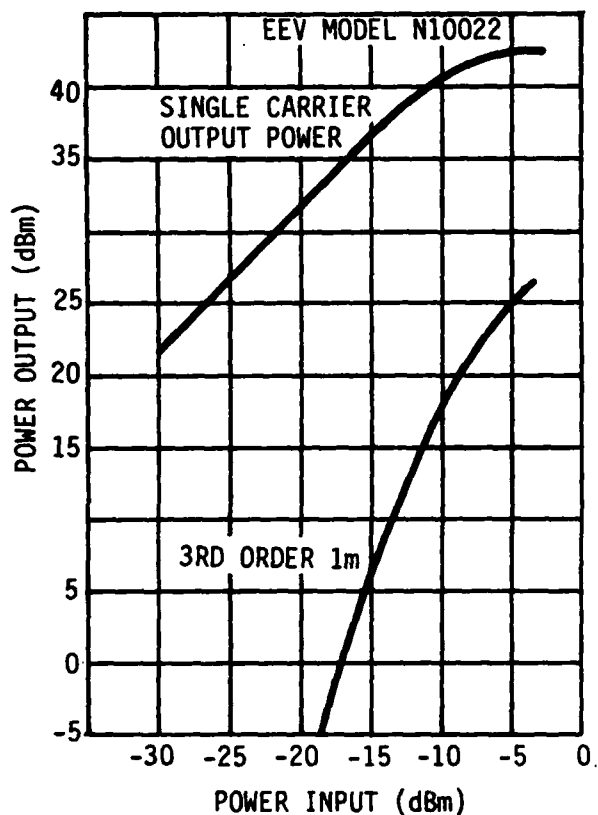
Figure 4-7 TWT AM/AM CHARACTERISTICS
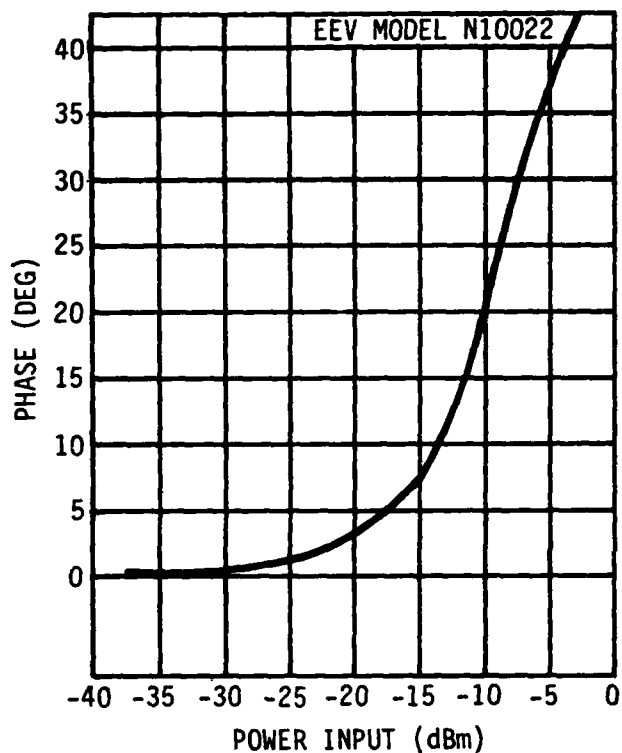
Figure 4-8 TWT AM/PM CHARACTERISTICS

4.5 IF FILTER AND AGC CIRCUIT

The AN/FRC-170(V) dual-diversity receiver simulation was composed of two identical receiver chains. Each included an IF and AGC section, modified Costas loop demodulator, three-level detection for QPR and two-level detection for QPSK, bit timing recovery, and data regeneration. Each receiver model has an IF and AGC section that preprocesses the received signal from the antenna using bandpass filtering and automatic gain controls. The IF filter model is a 6-pole bandpass filter with a variable bandwidth. The AGC circuit controls the baseband signal level by gain

and the modeled system has a dynamic range of 54 dB.

The simulated IF section for each receiver filters the IF signal plus noise and automatically controls the gain of the received baseband signal. Nominal values for the prototype modem's IF filter center frequency and bandwidth are 70 MHz and 40 MHz, which are 2681 Hz and 1532 Hz for the simulated filter. The IF bandpass filter simulated on the analog computer was programmed to model characteristics of Butterworth, Bessel, or Chebychev bandpass filters up to six poles. User programs have been developed to permit parameter changes for filter type, bandwidth, center frequency, ripple factor, and filter order.
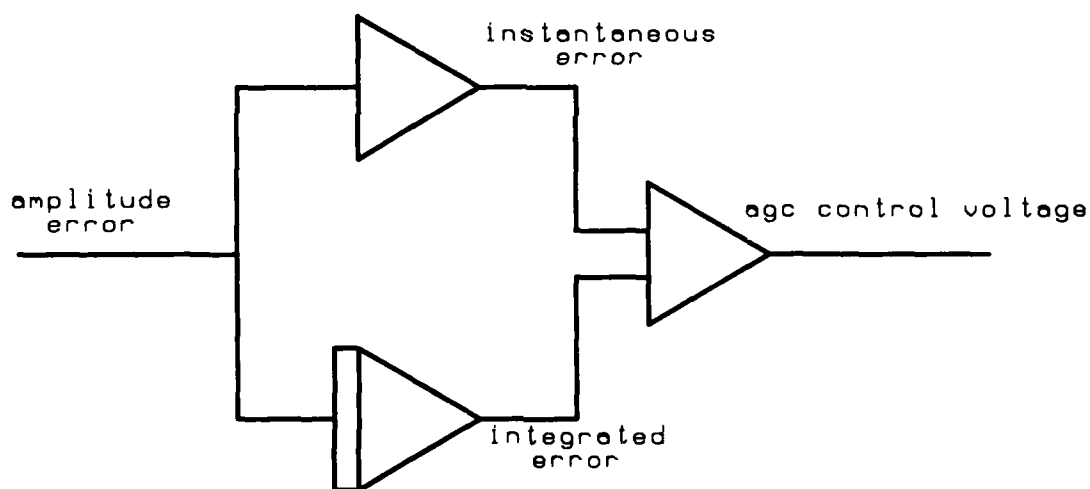
Figure 4-9   AGC LOOP FILTER

The AGC circuit rectifies the IF signal and filters it with a low-pass filter to detect the IF amplitude. The error between this amplitude and the nominal value is produced. This error is then applied to the AGC loop filter that sums the instantaneous error and integrated error as shown in Figure 4-9. This summation is the gain which the IF signal is multiplied by to achieve the nominal amplitude. The nominal value of amplitude is 25 volts. The dynamic range of the AGC circuit is 54 dB.

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4.6 MODIFIED COSTAS LOOP DEMODULATOR

The AN/FRC-170(V) radio uses a coherent demodulation technique which makes hard decisions on the filtered baseband and detects cross channel contamination between the I and Q demodulated symbol streams to phase lock a voltage controlled oscillator. This method of demodulation uses a modified Costas loop to extract the modulating signal. By multiplying the received IF signal with the in-phase and quadrature components of the phase locked reference oscillator, the two symbol streams (I and Q) can be detected. Outputs of the I and Q demodulators drive partial response, low-pass filters. The phase lock loop uses a cross correlation between the quadrature symbol streams low-pass filter outputs and hard decision estimates to generate a phase error signal. A difference of the resulting cross correlations is filtered and input to the reference VCO to phase lock it to the modulated carrier. The data estimation circuits provide two-level decisions for QPSK and three-level decisions for QPR.

New design data for the carrier recovery phase lock loop filters have been incorporated into the AN/FRC-170(V) radio simulation. Separate filters for lock and acquisition modes of the phase lock loop are now selected based on the receiver's "lock" indicator. In the lock mode, a narrowband filter is selected. In the acquisition mode, the carrier VCO is slaved to the modulator crystal controlled VCO and a wideband filter is selected. Both the narrowband and wideband PLL filters are Type I second order improved types. The circuits and transfer functions of these loop filters are given in Figure 4-10.

$$H(s) = \frac{R3 \times (1 + S \times R2 \times C)}{R1 \times (1 + S \times (R2+R3) \times C)}$$
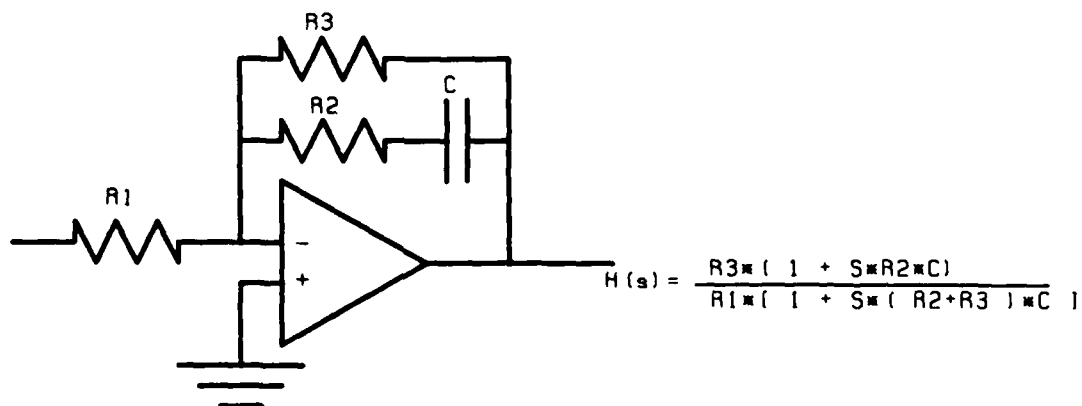
Figure 4-10   CARRIER PHASE LOCK LOOP FILTER

Identical demodulators with modified Costas loops were simulated on the analog computer for each of the dual diversity receivers. This circuit coherently demodulates either QPSK or QPR transmission, depending on the modulation technique selected. The demodulator modeled on the analog computer is shown in Figure 4-11.

Demodulation of the IF signal was simulated by using analog quarter square multipliers to multiply the received IF and phase locked reference to recover the baseband signal. The demodulated baseband is then low-pass filtered to remove the double frequency components resulting from the multiplication. The low-pass filters are 5th order elliptical type and are used for both QPR and QPSK.

These filtered baseband signals drive the data estimation circuits and cross channel I and Q multipliers. Data slicers for the data estimation and data recovery circuits were mechanized using analog
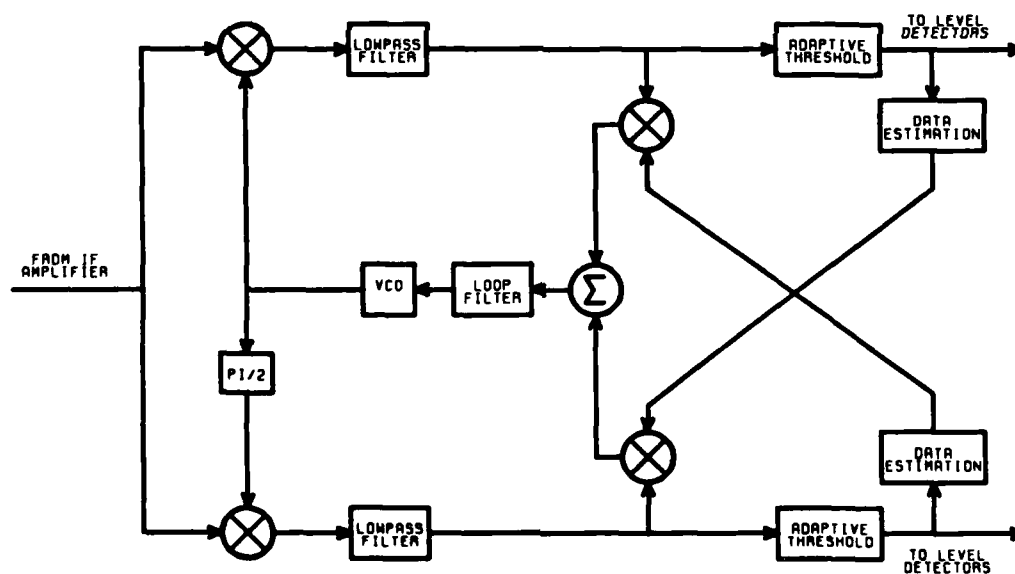
Figure 4-11 DEMODULATION MODEL

comparators to determine upper and lower for QPR, and center for QPSK. Baseband adaptive threshold circuits were programmed on the analog computer and used to optimally determine slicing levels for carrier and clock threshold detecting either QPR or QPSK. The hard decisions from the data estimations of the I and Q basebands were +1, 0, and -1 for QPR.

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Cross-coupling contamination products were obtained from the multiplication of the filtered baseband I and Q signals and an estimation of their value. The resulting signals were differenced using a summing amplifier on the analog computer and filtered by the appropriately selected narrowband or wideband PLL filters.

The optimum slicing level for data recovery, carrier recovery and the data clock is maintained using an adaptive threshold circuit. The system diagram for this circuit is shown in Figure 4-12. In the presence of noise and/or a fading channel the adaptive threshold derives an optimum slicing level by maintaining on an average a 50 percent duty cycle for the recovered clock.

The analog mechanization of the adaptive threshold was determined using reasonable approximations of the system circuitry, except for the highly coupled section that determines the data recovery slicing levels. This enhancement is based upon the actual circuit equations, thereby assuring that affects of the coupling are accurately simulated.

The narrowband and wideband carrier recovery Phase Lock Loop filters were simulated as one composite filter whose time constants were controlled by the acquisition/lock detector. These filters were mechanized using analog amplifiers, electrically controlled switches, and attenuators. Nominal time constants and gain for the wideband filter were T1=29.53, T2=0.5484 and A=30.42, and for the narrowband filter were T1=5958.8, T2=4.178 and A=26.83. The simulation of the composite filter is shown in Figure 4-13.

4.7 TWO AND THREE LEVEL DETECTION

To accommodate either QPSK or QPR, required both two-level and three-level detection of the baseband data. For QPR, each of the demodulated I and Q baseband signals were input to the adaptive threshold circuits and combined with slicing level coefficients to form the upper and lower slicing levels. These slicing levels and the baseband signals were input to comparators for detecting the presence of +1, 0, and -1 data from the demodulated baseband signals. For QPSK, the slicing coefficients were set to zero, and only the upper comparator is used to detect the binary baseband +1, and -1. Nominally, slicing levels are set to 50 percent of peak amplitude of a baseband signal to obtain optimum detection.

4.8 RECEIVER CLOCK RECOVERY

The bit timing recovery circuit provides synchronization for the data recovery circuits. Separate clocks are recovered for each of the two baseband signals, I and Q.

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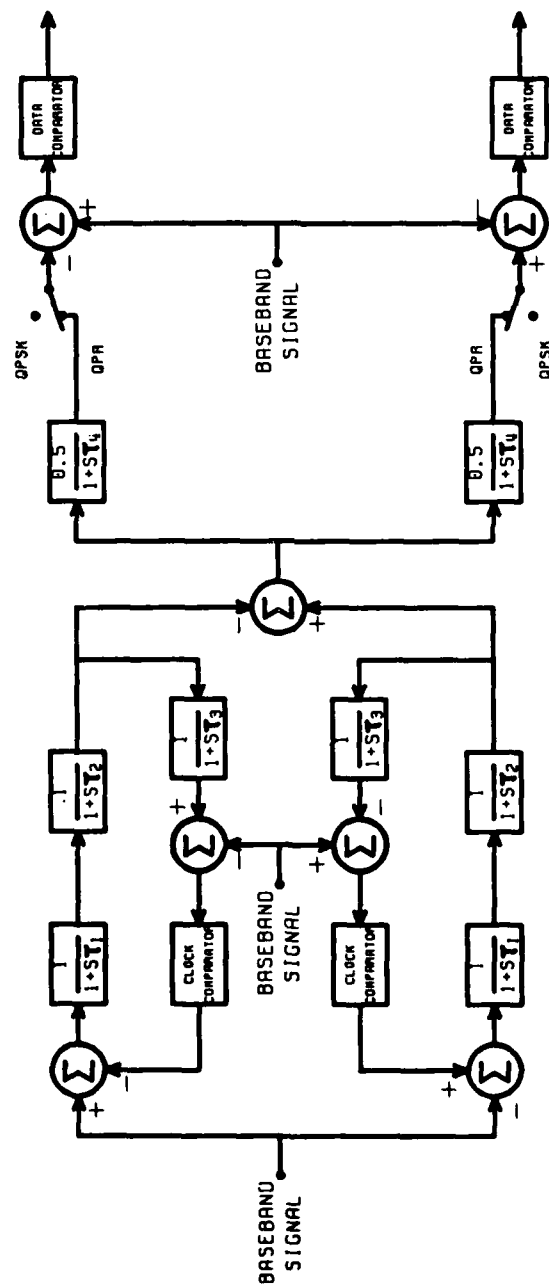
Figure 4-12   ADAPTIVE THRESHOLD SIMULATION DIAGRAM
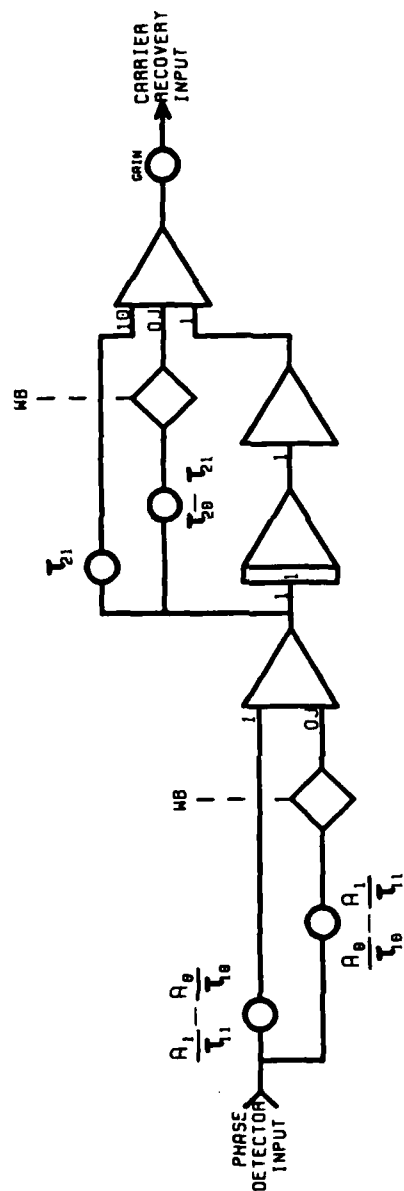
Figure 4-13   CARRIER RECOVERY PLL FILTER - ANALOG SIMULATION

The clock comparators compare the baseband signals to threshold slicing levels which are derived from the adaptive thresholds. This comparison provides an indication of data transitions. These data transitions are exclusively or'ed with the clock outputs to produce phase error signals. These signals drive D/A switches whose outputs are input to the phase detector amplifiers. The schematic and simulation diagram of the phase detector amplifier is given in Figure 4-14.

$$A = \frac{R_3}{2R_1}$$

$$T_1 = \frac{R_1 C_1}{2}$$

$$Y = A(E_1 - E_2)\left(\frac{1}{1 + T_1 S}\right)$$
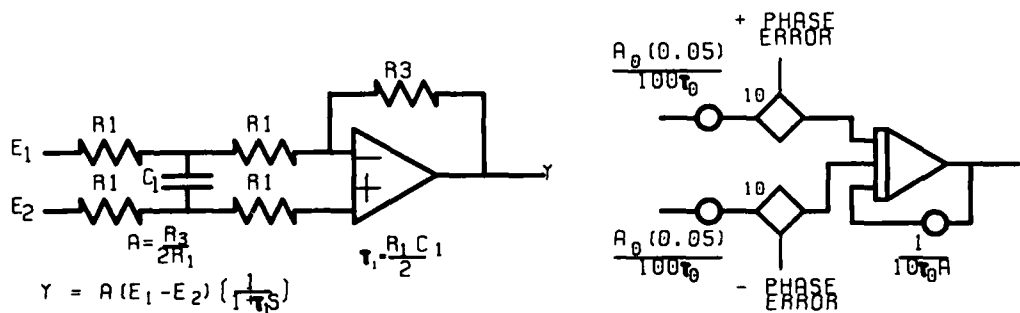
Figure 4-14 CLOCK PHASE DETECTOR AMPLIFIER MODEL

The outputs of the phase detector amplifiers are processed by narrowband Type 2 second order filters if the carrier is in a lock state. When the carrier is in acquisition mode, a wideband Type 1 filter is electronically selected. Nominal time constants for these filters are for narrowband T1=146.2 and T2=47.0 and for wideband T1=47.47 and T2=1.295 with a gain, A=100.56. Transfer function and circuits for these filters are shown in Figure 4-15.

The A clock output and B clock output are exclusively or'ed to provide an indication of clock synchronization. This signal drives the sync amplifier. When the output of the sync amplifier is above a set threshold, a LOCK signal is produced by a difference amplifier. This LOCK signal controls the selection of the wideband or narrowband clock recovery PLL filters discussed above.

The outputs of the clock recovery PLL filters are applied to the A and B clock VCO's, which drive the VCO's into the frequency and phase lock with the recovered clock. A block diagram of the clock recovery loop is shown in Figure 4-16.

$$H(s) = \frac{R_3}{R_1} \frac{[1 + SR_2C]}{[1 + S(R_2 + R_3)C]}$$
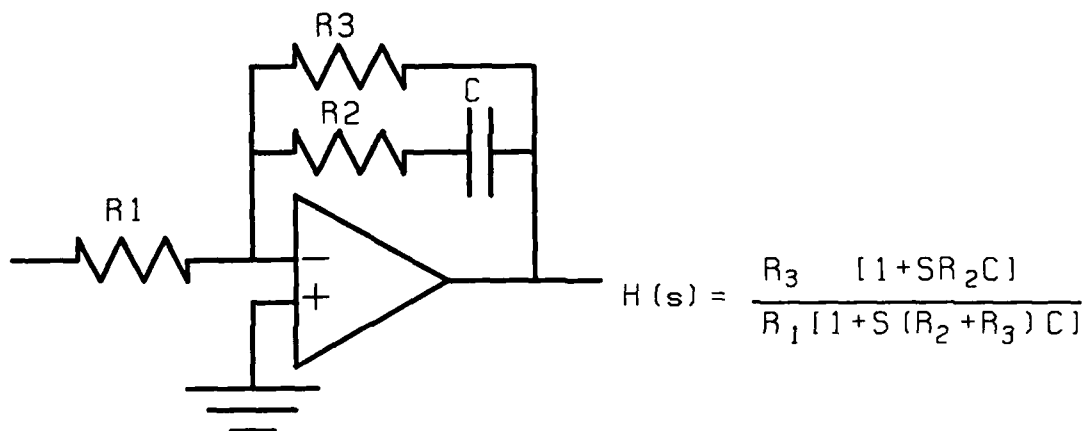
WIDEBAND, TYPE 1, SECOND ORDER IMPROVED

$$G(S) = \frac{1 + SR_2C}{SR_1C}$$
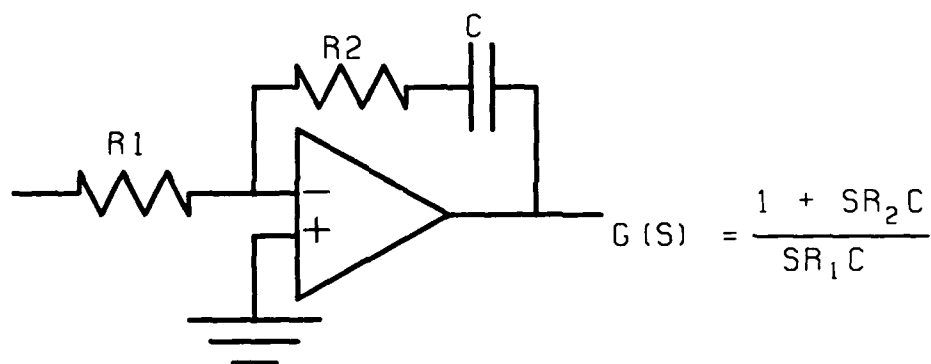
NARROWBAND, TYPE 2, SECOND ORDER

Figure 4-15   CLOCK RECOVERY PLL FILTER MODELS
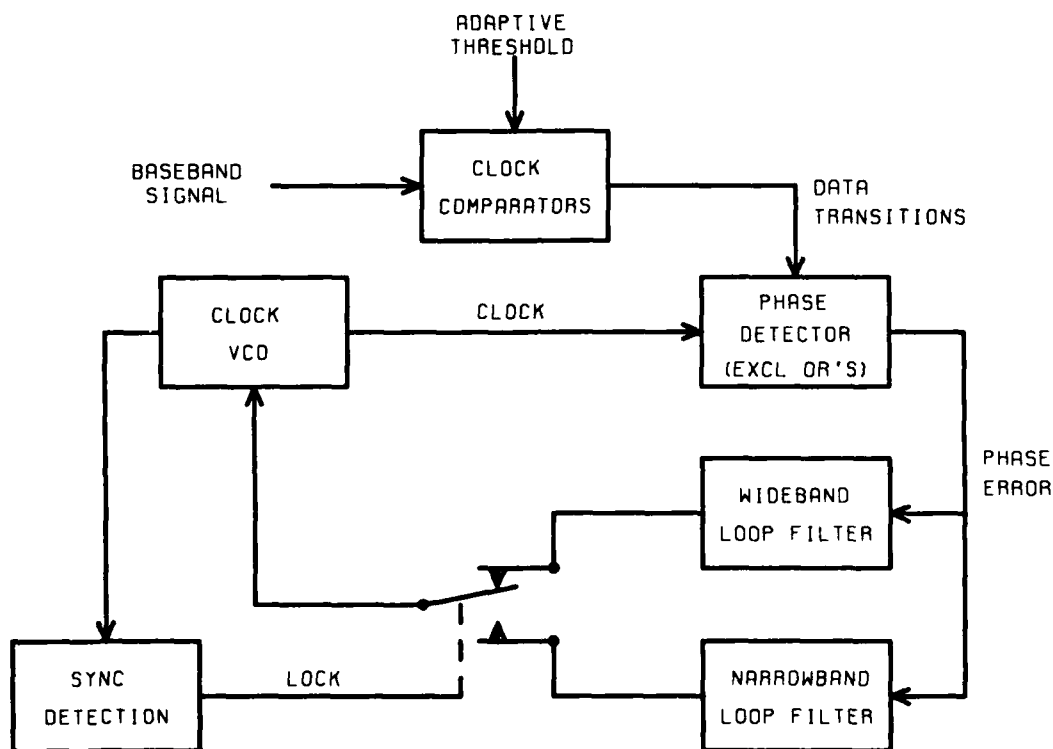
Figure 4-16 CLOCK RECOVERY LOOP DIAGRAM

4.9 DATA REGENERATION AND DESCRAMBLING

The detected two or three level baseband data is then sampled by the synchronized receiver clock for both in-phase and quadrature channels. For QPR, the sampling thresholds are determined by the adaptive threshold circuits. In QPSK, both bit streams are then passed through differential decoders. The bit streams are then recombined to form a single serial bit stream. A 20 stage self-synchronizing descrambler is used to reconstruct the original data bit stream. A block diagram of the data regeneration and descrambling is shown in Figure 4-17.
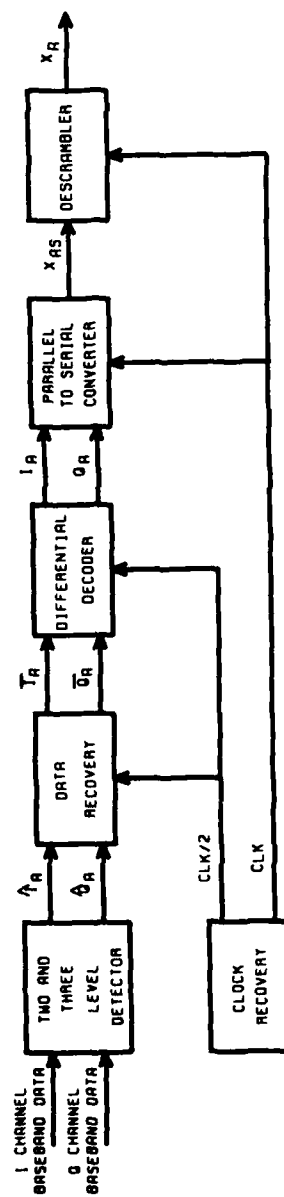
Figure 4-17 DATA REGENERATION AND DESCRAMBLING

5. RADIO EQUIPMENT ENHANCEMENTS

5.1 DECISION DIRECTED FEED-FORWARD AND FEEDBACK BASEBAND EQUALIZER

Section 5.1 and its sub-parts contain descriptions of the decision directed feed-forward and feedback equalizer, hereafter to be referred to as the BBE. Block diagrams, algorithms, equations, recommendations and results pertaining to the BBE are included. The equalizer is comprised of two forward taps in the feed-forward section and four taps in the feedback equalizer section. The algorithm used in the BBE is based on the minimum absolute value error forcing concept.

5.1.1 BBE PURPOSE AND CONCEPT

The BBE is a piece of hardware designed to eliminate intersymbol interference caused by multipathing effects in a line-of-sight channel model. The equalizer is designed to estimate the effects of the multipathing and to minimize them by introducing into the demodulated baseband countering *effects in a complementary fashion*. The basic design of the equalizer is based on documentation received from TRW Electronic Group of Redondo Beach, CA . Several modifications to the system were required to yield suitable performance. Modification evaluations were performed on the hybrid simulation model directly, allowing quick appraisals of various alternatives.

5.1.2 BBE ALGORITHM OVERVIEW

The BBE is of the decision directed feed-forward and feedback error correlation type. A reading of the baseband level is made at sampling time with a 6 bit A/D converter. Many readings will have errors associated with them due to channel noise and/or multipathing. There are 3 ideal states associated with the baseband sampling instant. The 6 bit A/D converter would yield outputs of -24, 0, or +24 for the three ideal states of -1, 0, or +1 respectively. A prom takes the A/D output which has been modified with correction factors and uses this value as its input address. The address points to an estimation of the baseband ideal state, (-1, 0, or +1). The prom, (called the data estimation prom), then yields as its output that estimation, (-1, 0, or +1) pointed to by its input address. The estimated state of the baseband reading will be that state whose ideal A/D conversion would be closest to the actual A/D reading. The error mentioned earlier is then the difference in the two values. This error is then correlated with past and future baseband values stored in analog and digital delay lines. If correlations are found with any of the non-present values, percentages of the non-present values are subtracted or added to the present value to eliminate the correlations due to non-present value contaminations in the channel. With each non-present value is stored an individual contamination

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coefficient. The contamination coefficient is that fraction which multiplies the non-present contamination term to yield a value to subtract from the present value which eliminates the correlation with that non-present term. Each contamination coefficient is updated individually. At equalibrium, any contamination introduced in the channel due to multipathing would be subtracted out within the equalizer. Cross channel contamination which is I to Q and/or Q to I inter-mixing in the channel is also eliminated by the BBE in the same manner. There are additional paths within the equalizer which subtract out those distortions in the same manner as the common channel contaminations mentioned above.

A simplified model of the demodulation loop and equalizer connections is provided in Figure 5-2.

5.1.3 ERROR ESTIMATION

Both the feed-forward equalizer, (FFE), and the decision feedback equalizer, (DFE), are functions of the error estimate algorithm, therefore the error algorithm will be details prior to the FFE or DFE.

Figure 5-2 is an eye pattern of an undistorted QPR signal. Note that at the SYM times which are the symbol sampling instants, there are 3 well defined crossover points. The lower, middle, and upper points correspond to -1, 0, and +1 symbol values respectively. Ideally, at sampling time, the baseband would be at exactly one of these three values. This would yield a zero error. Since the mechanism which reads the baseband is a 6 bit device, there is a range of approximately 1.5% that would yield a zero error reading on the A/D device. According to the original algorithm submitted by TRW, a single error estimate is taken for each received bit and is used for correlation in both the feed-forward and feedback equalizers. After extensive tests were performed on the equalizer hybrid simulation model and results were studied, it was found that equalizer stability was greatly enhanced by estimating the error both before feedback equalization for use in the FFE and after feedback equalization for use in the DFE. The error estimate prior to feedback equalization is called FFEERR for feed-forward equalizer error. The error estimate after feedback equalization is called DFEERR for decision feedback equalizer error. All error estimates are confined to be -1, 0, or +1.
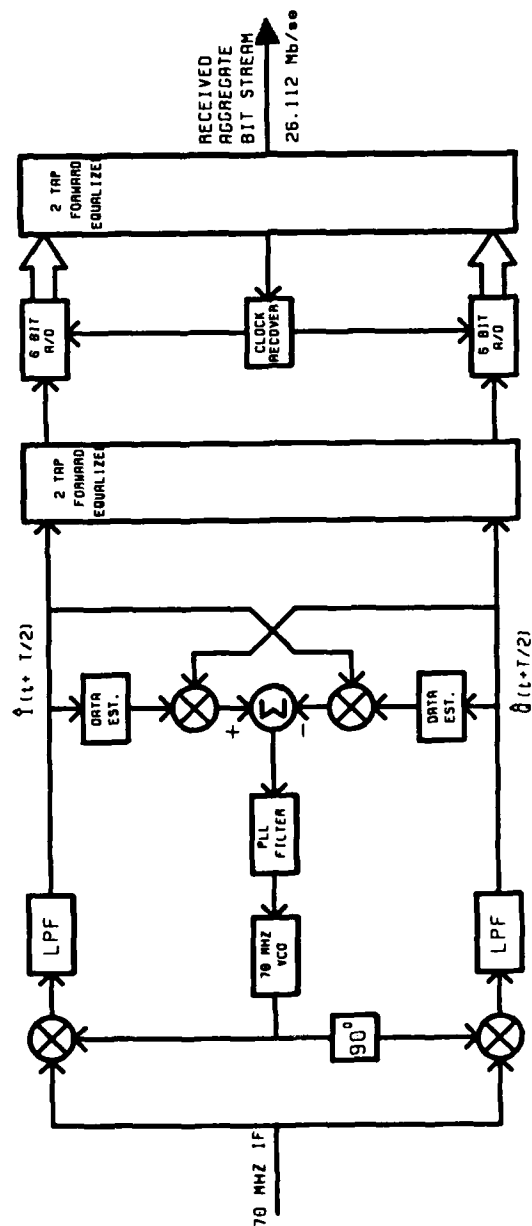
Figure 5-1   BASEBAND EQUALIZER AND DEMODULATION LOOP
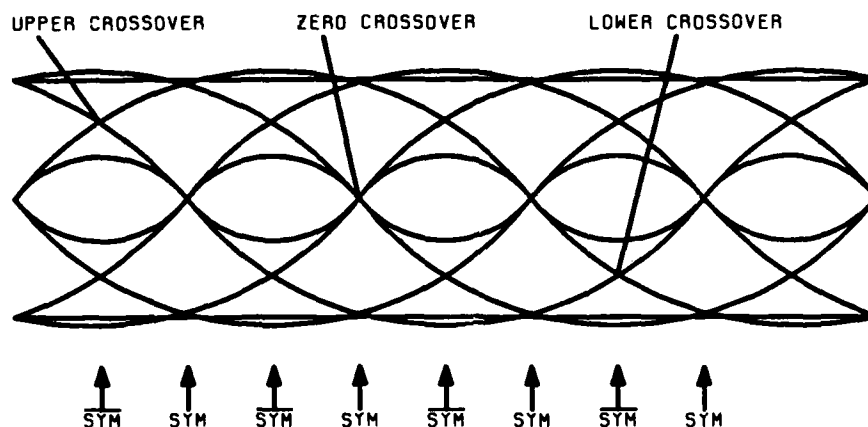
Figure 5-2 UNDISTORTED QPR EYE PATTERN

5.1.4 FFE DETAIL

As originally designed, the FFE was a three tap device as was proposed
in the statement of work. Further analysis by TRW indicated that the
performance enhancement to hardware complexity ratio was improved greatly by
the elimination of the third tap. Thus TRW modified the FFE to a two tap
device. The simulation model was also modified to contain two taps.

A block diagram of the FFE is supplied in Figure 5-3. As can be seen
from the diagram, the equalizer is symmetric in I and Q. I'FFE and Q'FFE
are used as inputs to the data estimation algorithm. IX and QX are used as
inputs to the clock recovery system. $I(t+T/2)$ and $Q(t+T/2)$ are inputs to the
error estimate correlation routines.
The following equations describe the makeup of I'FFE and Q'FFE:

$$I'FFE(t)=(1+CI0)*I(t)+CI1*I(t+T/2)+DQ0*Q(t)+DQ1*Q(t+T/2)-DEBIASI$$
$$Q'FFE(t)=(1+CQ0)*Q(t)+CQ1*Q(t+T/2)+DI0*I(t)+DI1*I(t+T/2)-DEBIASQ$$

47
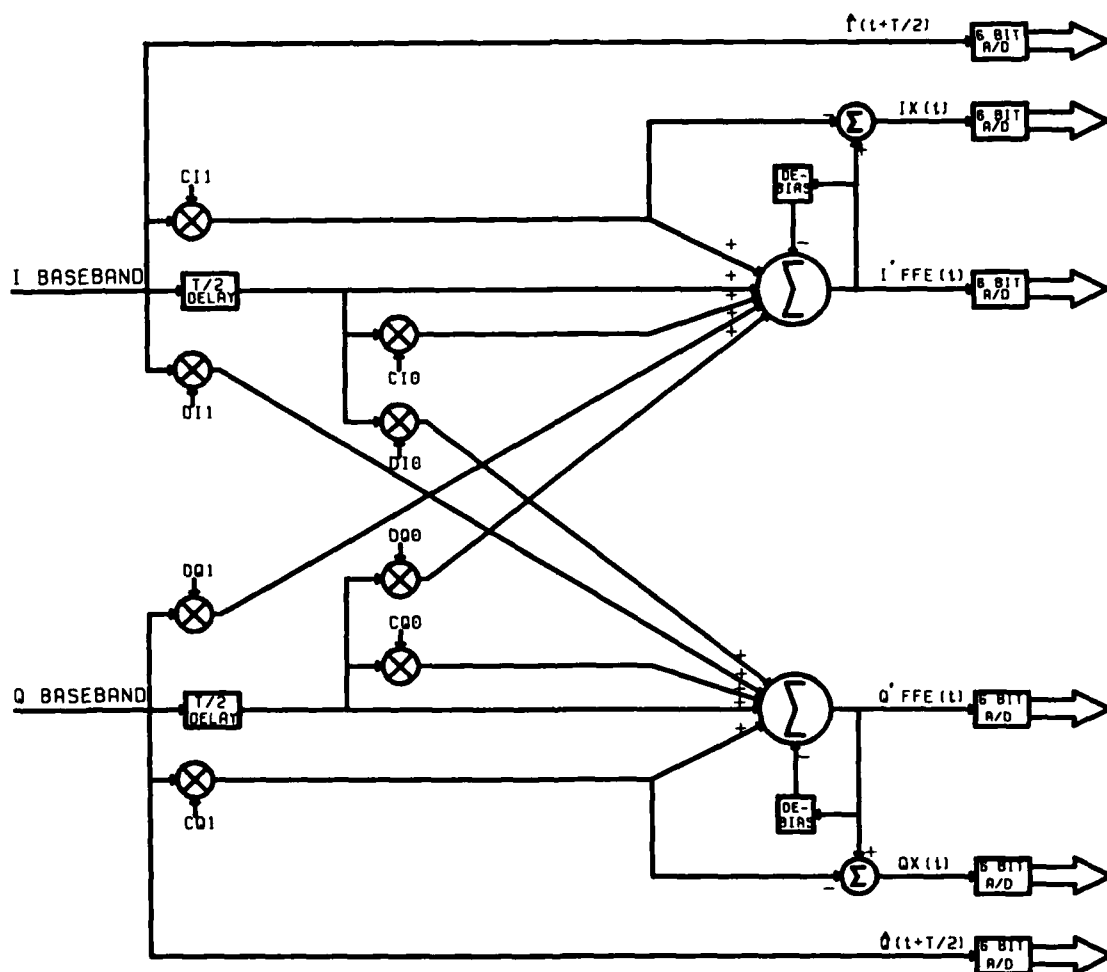
Figure 5-3 FEED-FORWARD EQUALIZER BLOCK DIAGRAM

The contamination coefficients in the above equations are CI0, CQ0, CI1, CQ1, DI0, DQ0, DI1, AND DQ1. Each channel has its own debias to counter biases created in the actual hardware.

Note the delay line providing the time delayed signals in the I and Q channels. The delay time used is one bit interval, or half of a baud interval. Fourth order Pade' approximations are used to implement the delays.

IX(t) and QX(t) are the same as I'FFE(t) and Q'FFE(t) respectively, except for the deletions of the common-channel undelayed terms. These are used for the clock recovery inputs. The TRW design uses the I'FFE and Q'FFE terms for clock recovery inputs. The simulation model indicated both clock and coefficient instabilities in using the TRW design.

All eight contamination coefficients update at the baud rate, the four coefficients serving the I channel on one bit and the four serving the Q channel on the next. The updates toggle between I and Q in the same staggered manner as the baseband sampling. Therefore they are updated at the baud rate and not at the bit rate. The following equations are used to update
the coefficients:

For k=0,2,4... :

$$CIO(k+1)=CIO(k)+FFEERR(k)*I(k)$$
$$CI1(k+1)=CI1(k)+FFEERR(k)*I(k+1)$$
$$DQ0(k+1)=DQ0(k)+FFEERR(k)*Q(k)$$
$$DQ1(k+1)=DQ1(k)+FFEERR(k)*Q(k+1)$$

For k=1,3,5... :

$$CQ0(k+1)=CQ0(k)+FFEERR(k)*Q(k)$$
$$CQ1(k+1)=CQ1(k)+FFEERR(k)*Q(k+1)$$
$$DIO(k+1)=DIO(k)+FFEERR(k)*I(k)$$
$$DI1(k+1)=DI1(k)+FFEERR(k)*I(k+1)$$

The debias circuits are analog high pass filters, an update submitted by TRW and implemented on both the real and simulated equalizers. The multipliers used to implement the various path gains are 8 bit multiplying D/A converters. The contamination coefficients are 16 bit quantities. This is an update from the initial 12 bit values implemented by both TRW and Martin Marietta in the simulation model. The 8 most significant bits of the 16 bit quantities are used as the inputs to the multiplying D/A converters. All signals are scaled such that if an overflow would occur in the actual equalizer, an overflow would also occur in the simulation model. Under normal circumstances, no overflows occur.

5.1.5 DFE DETAIL

Figure 5-4 is a block diagram of the DFE system. Note that all signals shown are digital with the number of bits representing each signal shown next to its location. I'FFE(t) and Q'FFE(t) are A/D converted to I'FFE(k) and Q'FFE(k). The multiplexer then toggles a selection between the two at the bit rate. The multiplexer output is then S'FFE(k), the 6 bit digital representation of the on-symbol FFE equalized baseband value. This value is then input to the error estimation prom to estimate the FFEERR value. This is the value used in the contamination coefficient update algorithm. The DFE correction factor, S'DFE(k) is then added to S'FFE(k) to produce S'(k), the final FFE and DFE equalized value.

Since S'FFE(k) and S'DFE(k) are both 6 bit quantities, the summation of the two can produce a 7 bit result, S'(k). S'(k) is then input to the data estimation prom to estimate the data value, (-1, 0, or +1). The data estimation prom also provides an error estimate, DFEERR which is used for DFE error correlation in its coefficient update routine.

The data estimation, S(k) is naturally a 2 bit quantity, 11 for -1, 00 for 0, and 01 for +1. The least significant bit then becomes the received bit. The two bit quantity, S(k), then enters a four bit delay line. The delay line contains S(k-1), S(k-2), S(k-3), and S(k-4). Percentages of these are combined to form the DFE feedback correction term, S'DFE(k). The term S'DFE(k) is developed slightly differently for an I bit, (k even) than during a Q bit, (k odd). The following equations are used :

For k=0,2,4... :

$$S'DFE(k) = +W1*S(k-1) + W2*S(k-2) + W3*S(k-3) + W4*S(k-4)$$

For k=1,3,5... :

$$S'DFE(k) = -W1*S(k-1) + W2*S(k-2) - W3*S(k-3) + W4*S(k-4)$$

The difference is due to the way the cross contamination is signed during demodulation because of the trigonometric relationships inherent to the system. The odd-delayed terms are cross channel terms and the even delayed terms are common channel terms. For example, if an I bit were being processed, S(k-1) would be Q(k-1), S(k-2) would be I(k-2), S(k-3) would be Q(k-3), and S(k-4) would be I(k-4). The W1, W2,
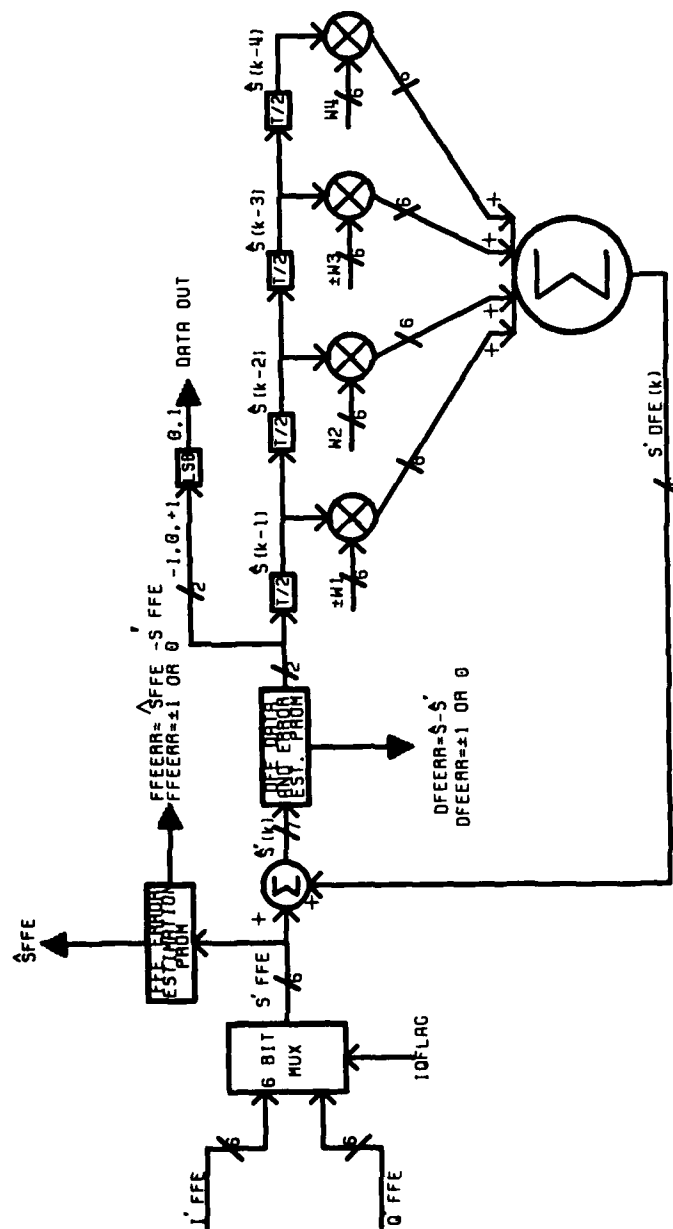
Figure 5-4 DECISION FEEDBACK EQUALIZER BLOCK DIAGRAM

W3, and W4 are contamination coefficients similar in function to the contamination coefficients explained in the FFE section. The W terms are 12 bit quantities, but only the 6 most significant bits are used in the multiplications. Since the S terms are either -1, 0, or +1, the sum of products expressed in the above equations, can be sums of +W or -W terms. For example:

assume k is odd, (Q)

assume $S(k-1) = +1$,
assume $S(k-2) = 0$,
assume $S(k-3) = -1$,
assume $S(k-4) = +1$

then

$S'DFE(k) = -W1 + W3 + W4$

This example shows how the multiplications are realized with a simple add or subtract, allowing much higher speed processing than if actual hardware multipliers were used.

The DFE coefficients W1, W2, W3, and W4 are updated at the baud rate. A slightly different set of equations are used during an I update than during a Q update.

For k=0,2,4... :

$W1(k+1) = W1(k) + DFEERR*S(k-1)$
$W2(k+1) = W2(k) + DFEERR*S(k-2)$
$W3(k+1) = W3(k) + DFEERR*S(k-3)$
$W4(k+1) = W4(k) + DFEERR*S(k-4)$

For k=1,3,5... :

$W1(k+1) = W1(k) - DFEERR*S(k-1)$
$W2(k+1) = W2(k) + DFEERR*S(k-2)$
$W3(k+1) = W3(k) - DFEERR*S(k-3)$
$W4(k+1) = W4(k) + DFEERR*S(k-4)$

The differences between I and Q processing arise again due to the trigonometry involved in the demodulation process.

5.1.6 BBE CLOCK RECOVERY

The BBE clock recovery is based on the "sampled crossover" concept developed by TRW. Clock stability is excellent with a center frequency maximum deviation of .01% . It was seen that performance was improved significantly by increasing the phase lock loop filter bandwidth by a factor of ten. This shortened lock detection time without degrading performance of the system after narrow band acquisition. Figure 5-5 is a block diagram of the BBE clock recovery loop.

The basic sensing algorithm used to determine if the clock is ahead of schedule or behind schedule is an examination of the sign (+ or -) of the present symbol and the sign of a symbol one baud earlier with the qualifier that the two symbols are not the same. For example, if both symbols are -1, then the test is skipped. If the two symbols are different, they will be of one of the sets listed below:

o -1 to 0

o -1 to +1

o 0 to -1

o 0 to +1

o +1 to -1

o +1 to 0

Note that the -1 to +1 and +1 to -1 transitions are illegal. The only way this transition could occur under normal circumstances is if the clock would be out of sync. If a transition of this type is detected, The PLL filters go into wide band mode and kicks the clock in a constant direction. This causes the clock to move in a constant direction till sync is re-attained.

The way the sensing routine works will be illustrated with an example. Please refer to Figure 5-6.

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Figure 5-5   CLOCK RECOVERY BLOCK DIAGRAM

UPPER CROSSOVER   ZERO CROSSOVER   LOWER CROSSOVER

X(k)

X(k-2)

SYM   SYM   SYM   SYM   SYM   SYM   SYM   SYM
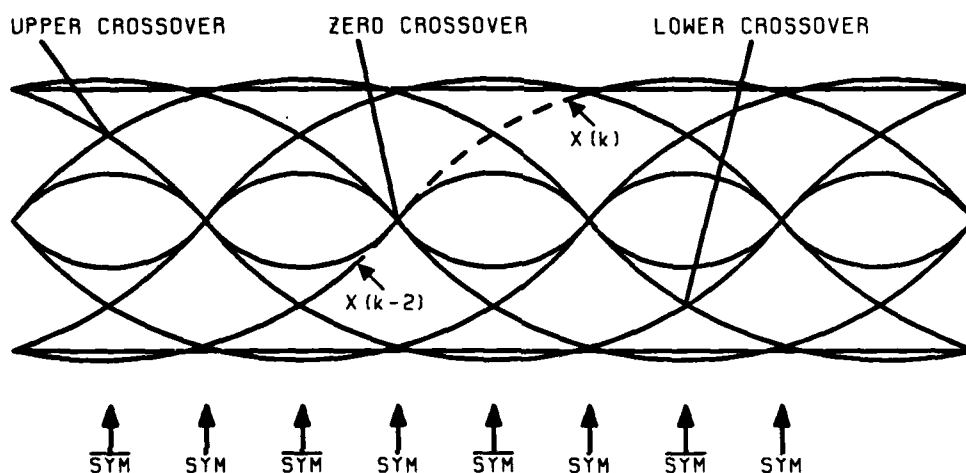
Figure 5-6   EARLY TIMING ILLUSTRATION

Note a transition from 0 to +1 has occurred, (S(k-2)=0, and S(k) =+1), and X(k-2) is a negative value. This indicates that the baseband was at a negative value at the time X(k-2) was sampled, and was travelling through zero on its way up to a +1. If X(k-2) had been read at the proper time, it would have been exactly zero. Since it was read early, it was still negative. The fact that the symbol value was 0 and its 6 bit representation was negative and it was travelling to a +1 state indicates the sample was taken too early. An inspection of Figure 5-6 will clarify why this is so. A similar type of situation exists for any of the other legal early or late transition samplings listed above.

As discussed in Section 5.1, IX(k) and QX(k) are the inputs to the clock recovery loop. Figure 5-7 is an expanded table of the contents of the crossover prom.

CROSSOVER PROM TRUTH TABLE

$\hat{S}(k)$	$\hat{S}(k-2)$	XMSB(k)*XMSB(k-2)	FASTER	SLOWER
-1	-1	0 OR 1	1	1
0	0	0 OR 1	1	1
+1	+1	0 OR 1	1	1
-1	0	0	1	0
-1	0	1	0	1
+1	0	0	1	0
+1	0	1	0	1
0	-1	0	0	1
0	-1	1	1	0
0	+1	0	0	1
0	+1	1	1	0
-1	+1	1	0	1
+1	-1	1	0	1

Figure 5-7   CROSSOVER PROM CONTENTS

5.2 IF BUMP AND SLOPE EQUALIZER

The IF bump and slope equalizer, (IFE) is situated between the output of the IF amplifier and input to the demodulator loop. The IFE is based on a servo loop mechanism, maintaining constant power levels in 3 individual spectral bands across the IF bandwidth.

A block diagram of the system is given in Figure 5-8. Prior to use, the IFE is automatically calibrated by the digital computer. At any time, the remote user will be able to initiate a re-calibration by entering the proper command.
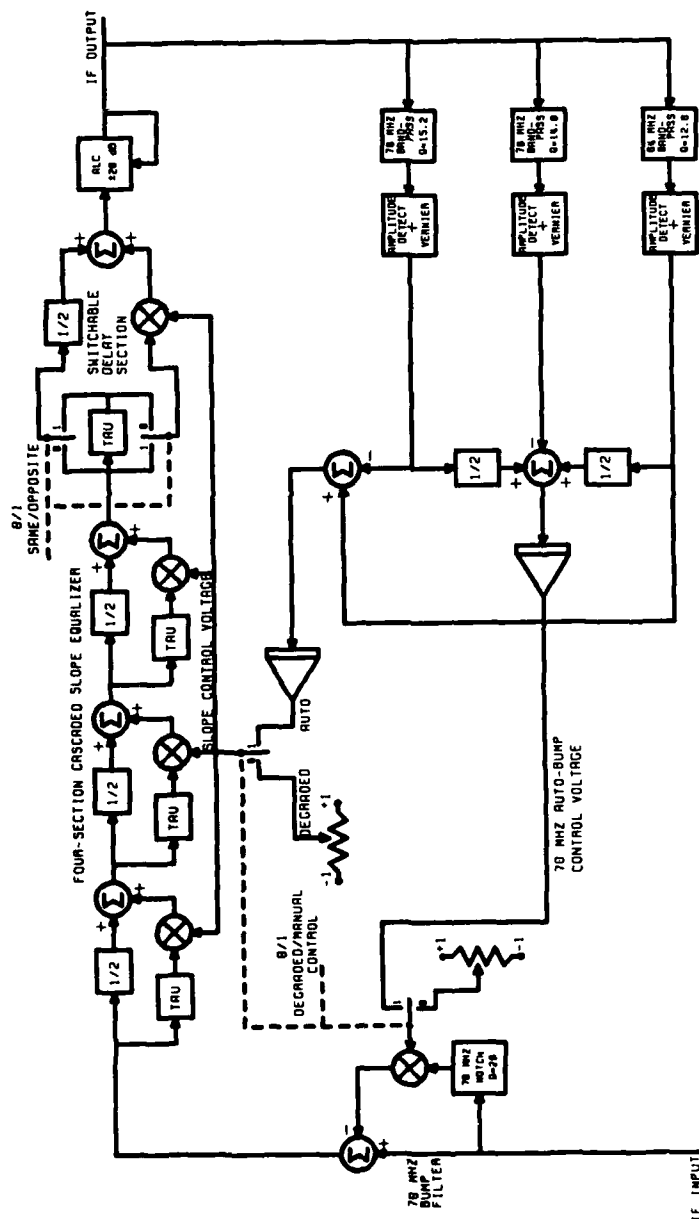
Figure 5-8   BUMP AND SLOPE EQUALIZER BLOCK DIAGRAM

There are basically 5 main sections to the IFE. They are:

I.   Bump Equalizer

II.   Slope Equalizer

III.   Automatic Level Control (ALC)

IV.   Power Detectors

V.   Coefficient Generators

These are arranged in the servo loop. Any error at the output of the loop (which would be the input to the demods) is used to drive the signal corrective circuitry in the rest of the loop. Error detection at the output of the loop is accomplished by feeding the output into 3 narrow band (5 MHz) amplitude detectors. The center frequencies are at 64, 70, and 76 MHz. Actually, the detectors sense the mean amplitude across each 5 MHz bandwidth since it's not, in general, constant. The gain of each amplitude detector is verniered to yield a nominal output of 50 volts. (The EAI 8800 analog computers are scaled to a 100 volt unity.)

Figure 5-9 is a schematic of the 64 MHz amplitude detector and vernier. All three detectors are similar except for center frequencies. Note that the frequencies are time scaled by 1/26112.

The outputs of the 3 amplitude detectors are then input to the coefficient generators. The coefficients are used to control the bump equalizer section and slope equalizer sections.

The time derivative of the slope equalizer coefficient is developed by taking the 76 MHz amplitude level and subtracting from it the 64 MHz amplitude level. If the difference is negative, the coefficient is increased by the following integrator, to yield a coefficient value sufficient to drive the original difference to zero. At this time, the derivative is zero and the integrator output does not change, allowing a proper control voltage with no error voltage.

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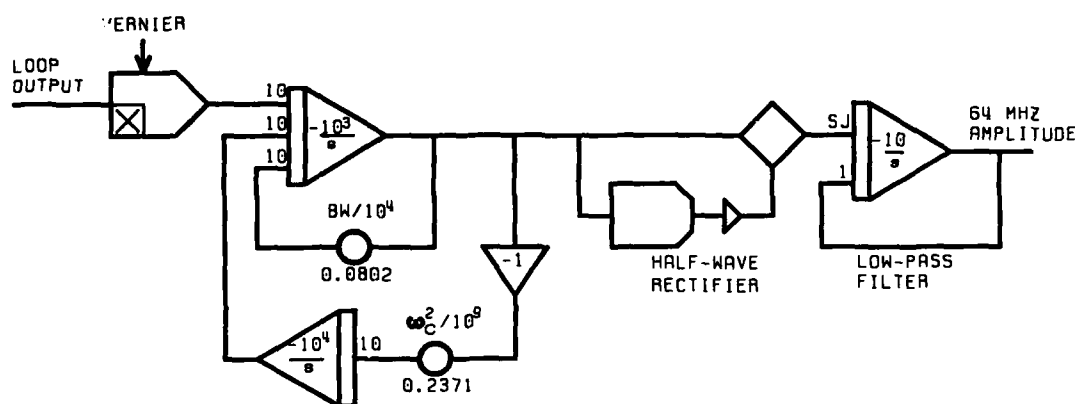
BANDPASS FILTER

Figure 5-9 64 Mhz AMPLITUDE DETECTOR

Alternatively, to force a reduced effectiveness, the coefficient may be selectively set by the digital computer to any percent of the nominal control voltage by throwing a relay and elimination the auto-slope control voltage. Figure 5-10 depicts the slope coefficient generator.

The slope control coefficient is used to control the characteristics of a variable filter. With a positive control coefficient voltage, the filter gives a positive slope frequency response. With a negative control voltage, the filter provides a negative slope characteristic. The intensity of the slope created is monotonically related to the magnitude of the control voltage.

The variable filter is comprised of 4 cascaded sections, all similar except for a phase characteristic reversal option on the last one. Figure 5-11 is a block diagram of the last two sections.

Figure 5-10 SLOPE CONTROL COEFFICIENT GENERATOR

Figures 5-12 through 5-14 are Bode plots of the filter for maximum negative slope, maximum positive slope and maximum positive slope with last stage reversed phase option, respectively.

Figure 5-11 LAST TWO SLOPE EQUALIZER SECTIONS

Each section of the slope equalizer works by summing the IF with a delayed version of the IF. The delay corresponds to a 270 degree phase shift at the IF center frequency. For the simulation, this mandates a 0.2794 msec. delay.

$$\left[\frac{1}{70 \text{ Mhz}}\right] * \left[\frac{270}{360}\right] = 0.2794 \text{ msec.}$$

60
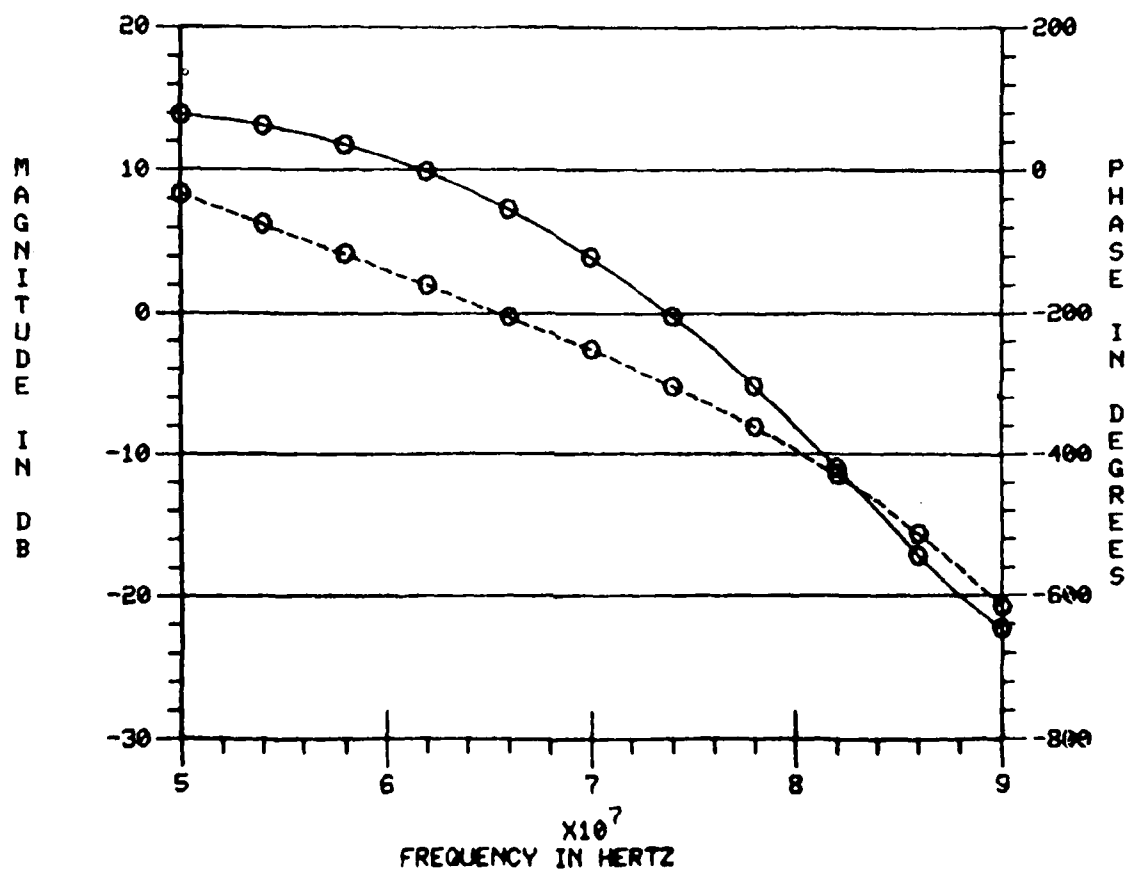
Figure 5-12   SLOPE EQUALIZER MAXIMUM NEGATIVE SLOPE
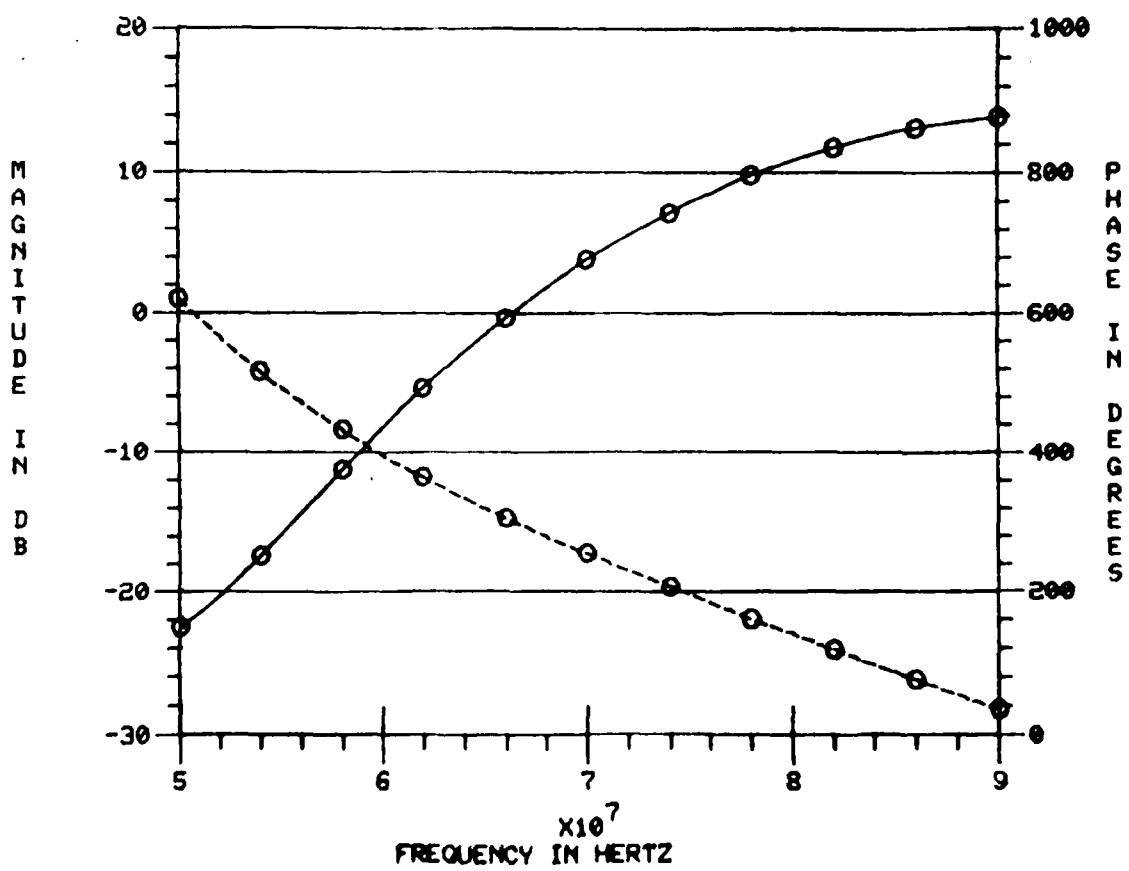
Figure 5-13   SLOPE EQUALIZER MAXIMUM POSITIVE SLOPE
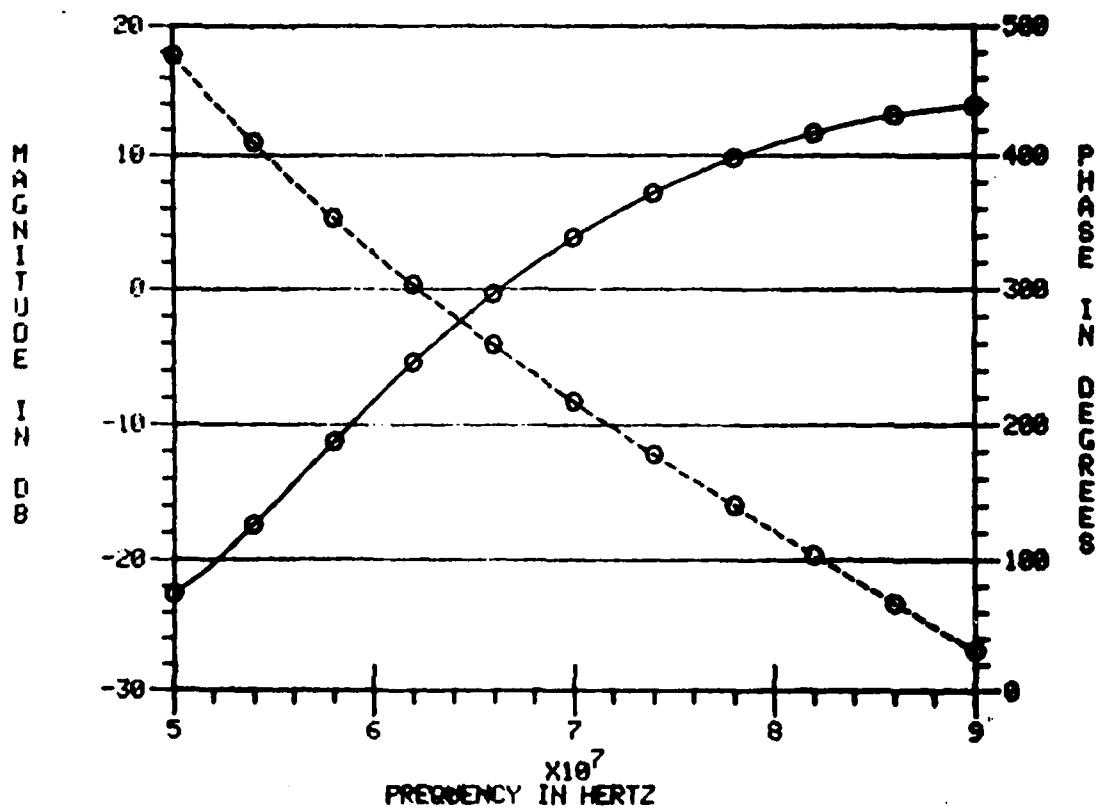
Figure 5-14   MAXIMUM POSITIVE SLOPE REVERSED PHASE

At 93.3 MHz, or 3573 Hz at scaled frequency, this represents 360 degrees while at 46.7 MHz or 1786 Hz at scaled frequency this represents 180 degrees phase shift, yielding positive slope throughout the spectral bandwidth. This situation arises with a positive slope control voltage. A negative slope control voltage would invert the delayed signal, and hence reverse the frequency gain characteristics centered around 70 MHz.

In review, the amplitude levels at the outermost two power bands are found with the amplitude detectors. These levels are used to develop a control voltage for the variable slope filter. The slope of the filter is controlled by altering the power levels across the IF bandwidth.

The slope equalizer section cannot in itself remove bumps or notches in the middle of the complete spectral bandwidth of the IF. As a matter of fact, due to the curvature of the slopes created by it, (as can be seen in the Bode plots), the slope equalizer can create a small excess of power at the center of the bandwidth. These problems are alleviated by the bump equalizer section.

The bump equalizer also works in a servo loop fashion. The amplitude detectors sense a bump or notch in power and develop a coefficient derivative. The derivative is integrated to develop a control voltage for the bump equalizer. The bump equalizer then adjusts the gain at its center frequency to compensate for the bump or notch.

The bump equalizer is centered at 70 MHz. The coefficient derivative is developed by use of the output of the 3 amplitude detectors. The coefficient derivative compares the amplitude level at 70 MHz with the average of its two adjacent power levels, 64 MHz and 76 MHz. The averaging is done by adding the two adjacent amplitude levels and dividing by two. Then the 70 MHZ level is subtracted off. Since the process is linear, the addition and subtraction is performed by summing the proper signals on one amplifier. The division is performed on the inputs rather than the output. This creates the coefficient derivative which is then integrated to yield the coefficient. The integrator serves the same purpose as the integration in the slope equalizer coefficient generator, that is, to allow error voltages to go to zero due to proper equalization and still maintain a control voltage to drive equalization. Figure 5-15 is a schematic of the 70 MHz coefficient generator.

$$\frac{-d\,(C70)}{dt} = (1/2\,(V_{64} + V_{76}\,) - V_{0}\,)$$
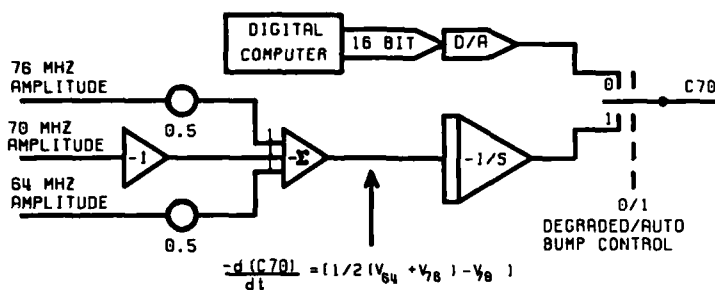
Figure 5-15   70 Mhz CONTROL VOLTAGE GENERATOR

The coefficient generated will range between +1 which would drive the bump equalizer to act as a bandpass *filter* and −1 which would cause the *bump* equalizer to act as a notch filter.

A block diagram of the 70 MHz bump equalizer is found in Figure 5-16. A schematic is shown in Figure 5-17.
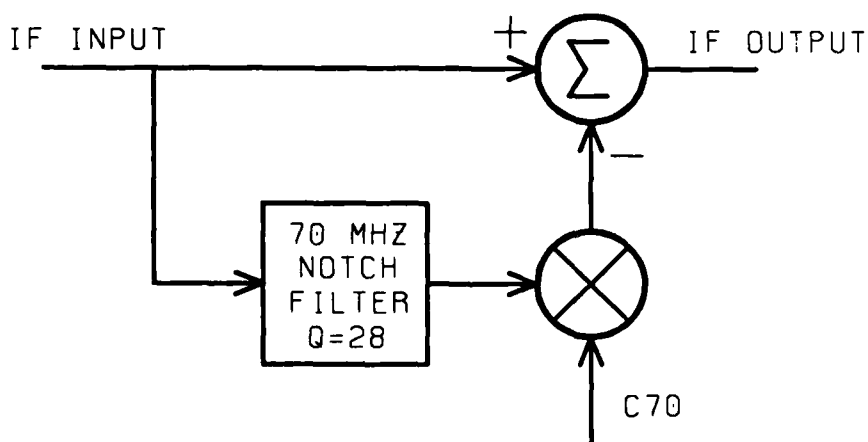
Figure 5-16   70 Mhz BUMP FILTER BLOCK DIAGRAM

The bump equalizer works by summing 2 paths. One path is straight through and one path goes through a sharp notch filter with a Q of 28. For the case of the 70 MHz bump equalizer, the notch would be at 70 MHz. Since the phase response of the notch filter is very nearly zero degrees everywhere but at the center frequency, constructive or destructive interference of varying degrees can be induced everywhere but at the center frequency by varying the filter path gain from +1 to -1. This can be seen by inspection of the accompanying transfer function for the complete two path section:

$$H70(s) = \left[\frac{(1-C_{70})\ s^2 + (w_c/Q)\ s + (1-C_{70})\ \omega_c{}^2}{s^2 + (w_c/Q)\ s + \omega_c{}^2}\right]$$

When $C_{70} = -1$ the filter acts as a notch filter. When $C_{70} = +1$ the filter acts as a band pass filter. Figures 5-18 through 5-21 show resulting Bode plots for cases where $C_{70} = -1$, $-.5$, $+.5$, and $+1$.

$$\omega_c = 2\pi \cdot \frac{70\ \text{MHZ}}{26112} = 15400$$
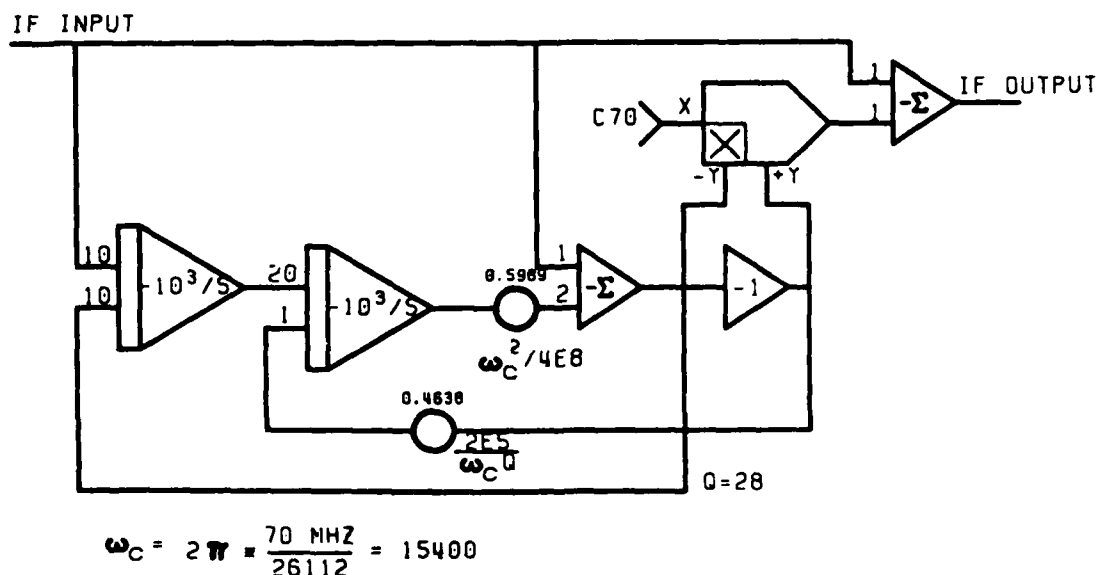
Figure 5-17   70 Mhz BUMP FILTER SCHEMATIC

66
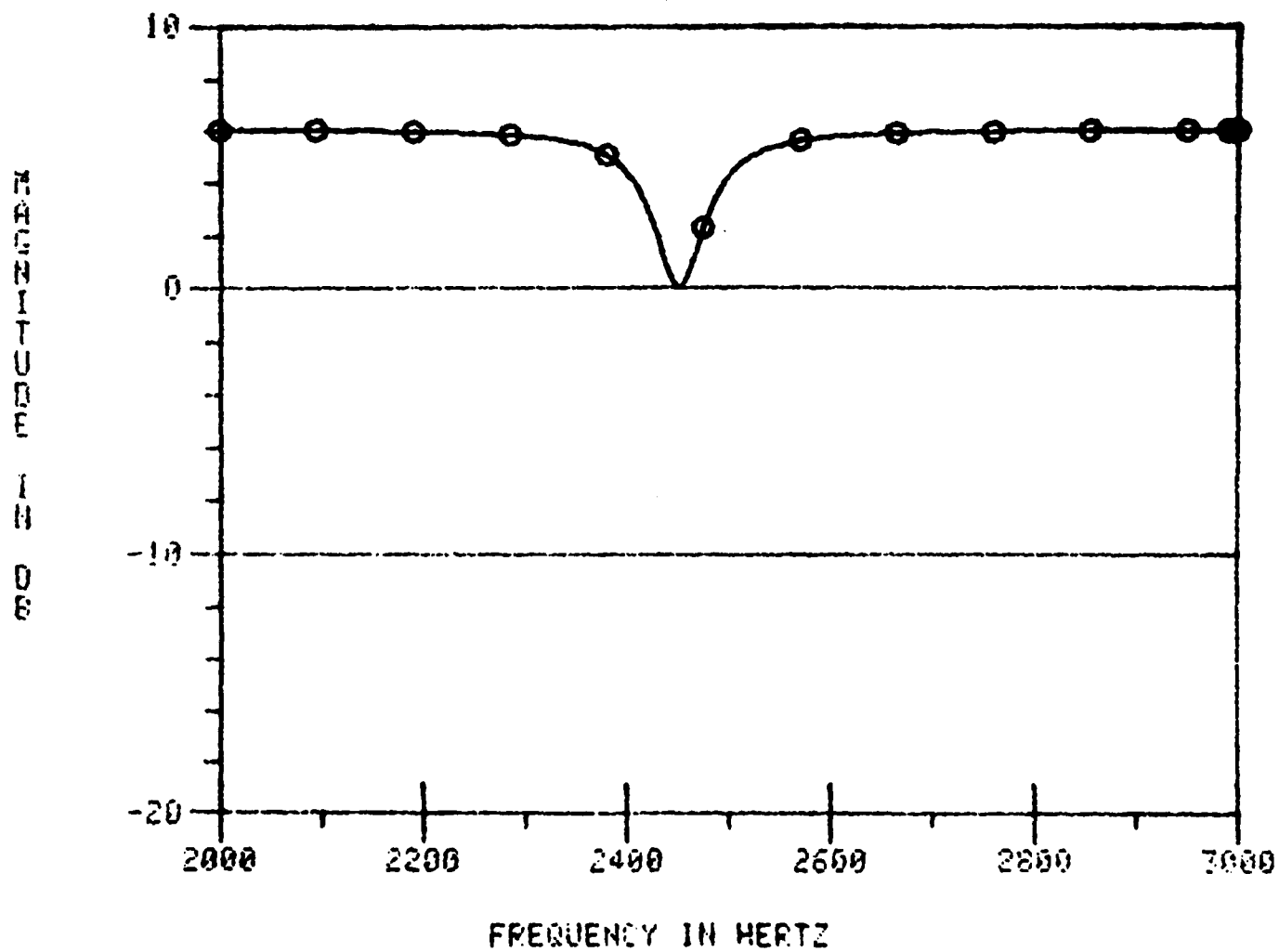
Figure 5-18 70 Mhz FILTER AT MAXIMUM NOTCH
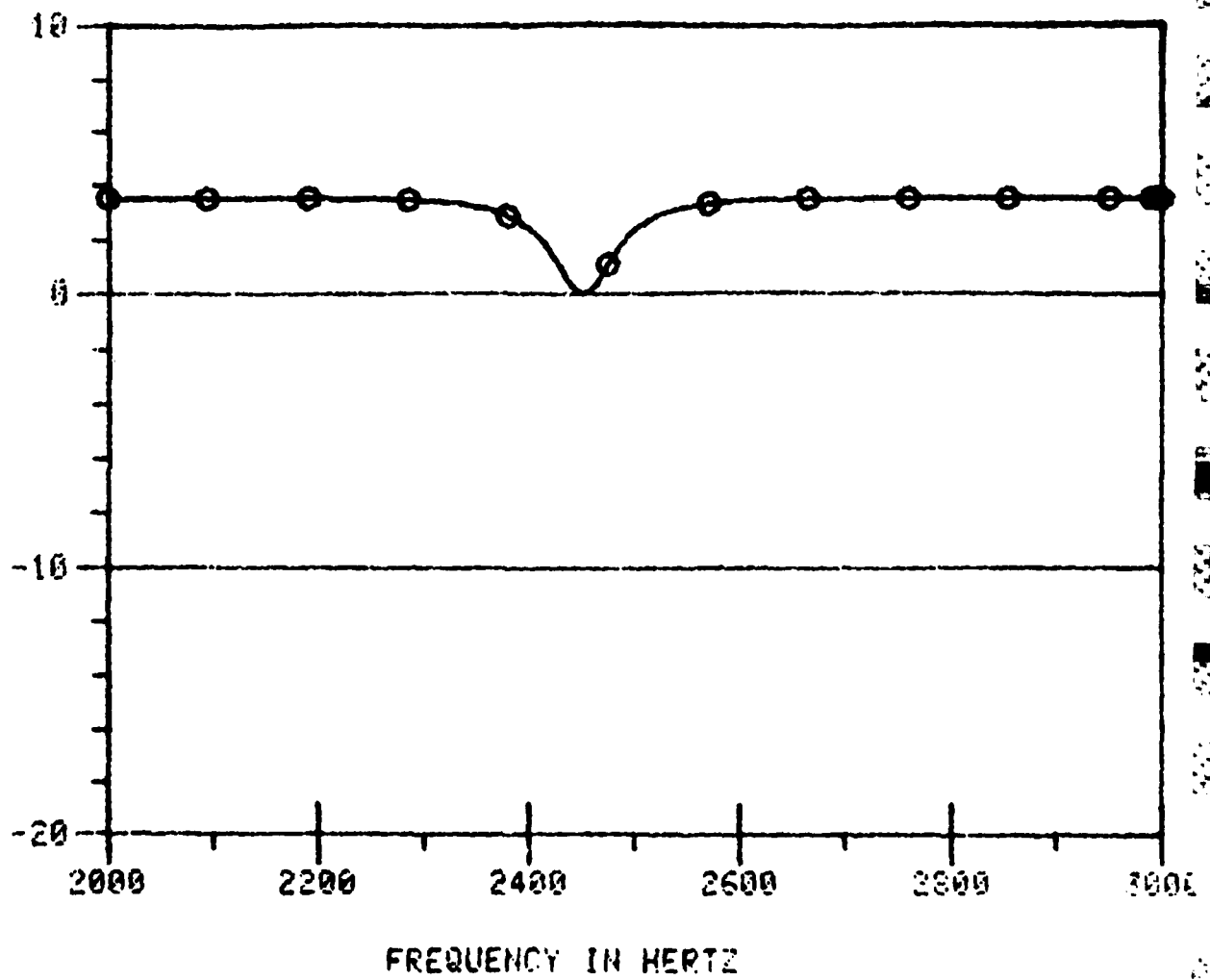
Figure 5-19   70 Mhz FILTER AT SEMI-NOTCH
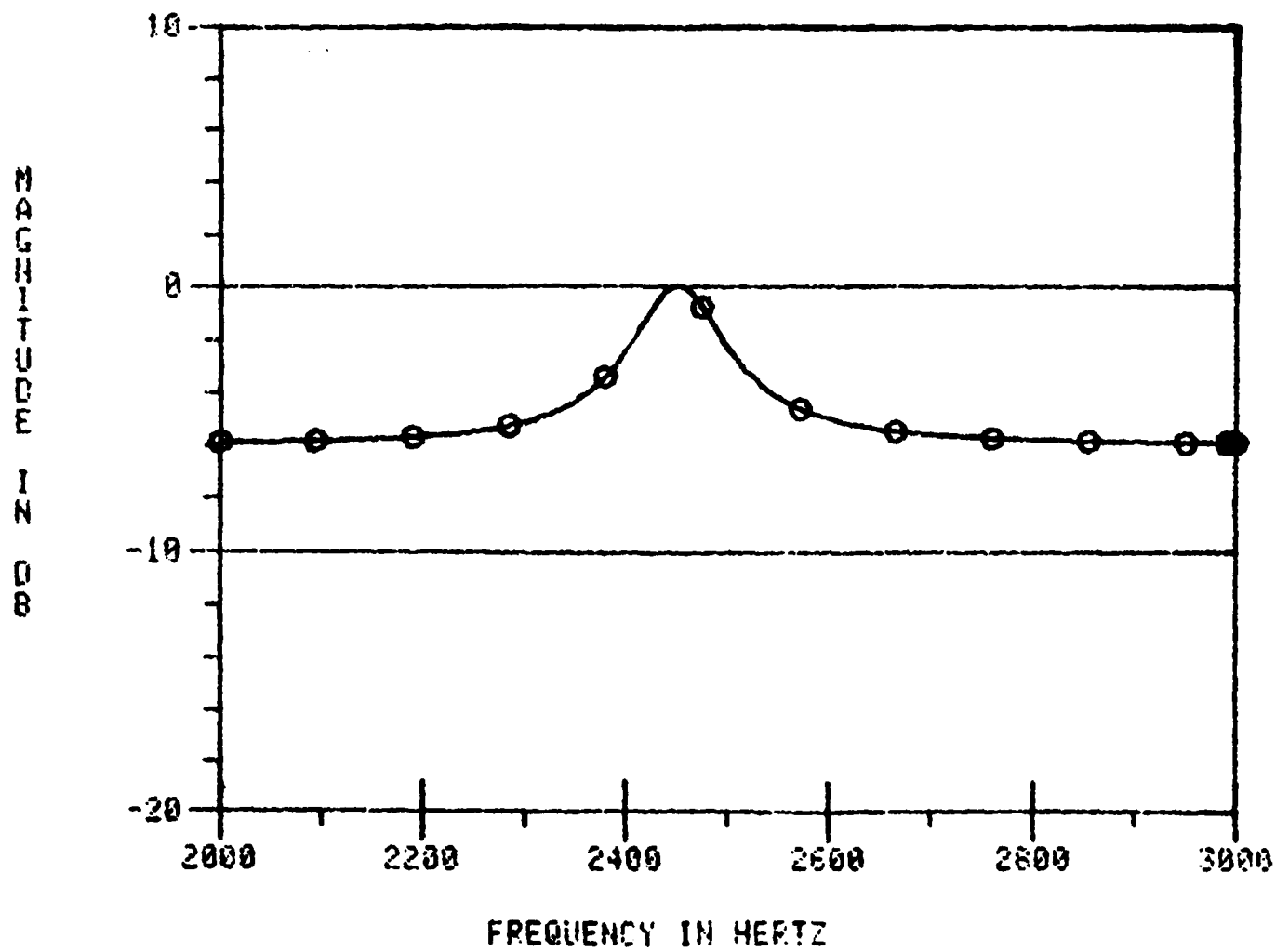
Figure 5-20   70 Mhz FILTER AT SEMI-BANDPASS
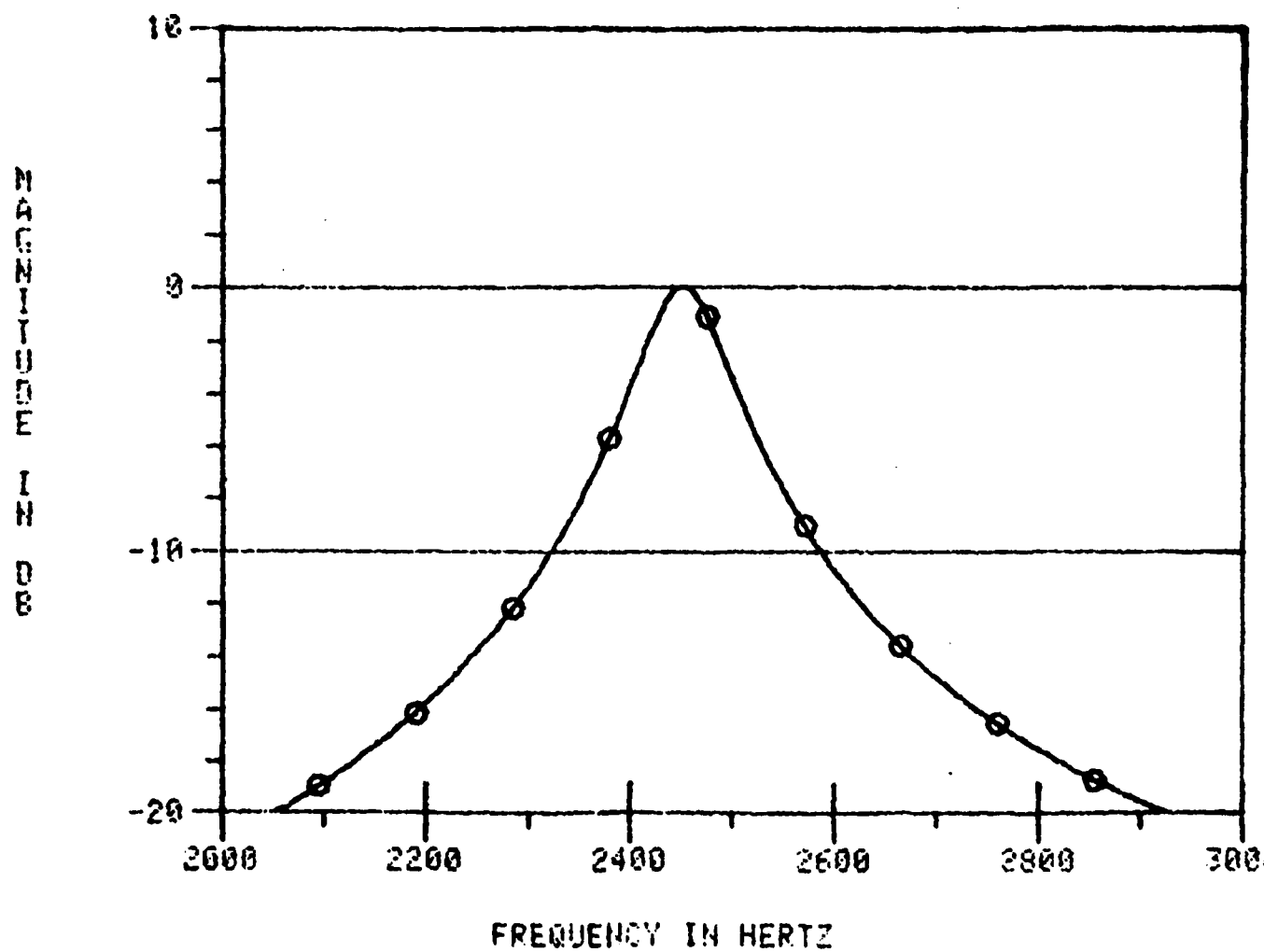
Figure 5-21   70 Mhz FILTER AT MAXIMUM BANDPASS

As can be seen from the Bode plots of the different equalizer sections, overall loop gain can be affected by trying to change the shape of the equalizers frequency response. This is remedied by the inclusion of the Automatic Level Control, or ALC. The ALC is identical to an AGC circuit. The ALC can produce +20 dB of gain compensation.

The performance of the IFE correlated well with anticipated theoretical results. Still, it was apparent that a single bump equalizer was not sufficient. A three bump approach would yield a more desirable margin of improvement. Initial studies indicated that a three bump approach would require more research time and development, thus subtracting from the analysis time allotted to studying the advantage of any IF equalizer.

5.3 TDM FRAME SYNCHRONIZATION SUBSYSTEM

The output of the TDM transmitter is organized into frames, where a frame length, defined as the super frame, of N bits consists of a known framing pattern of 16 bits, which was implemented as a result of contract DCA 100-81-006, and N-16 information bits. An automatic frame counter which is always correct keeps a count of the bits in the super frame, cycling between 1 and N bits. A specified framing pattern of ones and zeros is inserted periodically into the transmitter bit stream.

The TDM receiver acquires and maintains frame synchronization through the use of a maintenance mode and a search mode. The initialization mode and output mode are support algorithms that are used in TDM analysis. Also included as part of TDM is the TDMINT algorithm which is used in sync acquisition time analysis. The remainder of this section will give a description of the four basic modes of TDM operation, and the TDMINT algorithm.

5.3.1 INITIALIZATION MODE

The initialization mode is entered by typing the $TDM command. The user is prompted to input receiver A or B, the up-down counter size, the 16 bit framing pattern, the number of errors acceptable for maintenance mode correlation, the number of errors acceptable for search mode correlation, and the down count increment. The down count increment is the value by which the up-down counter is decremented. A sample initialization sequence is shown in Figure 5-22. User entry is in *ITALICS*, computer response is in **BOLD**. Immediately prior to a test, the framing is synchronized in a controlled fashion to keep initial synchronization statistics from affecting run time statistics. After synchronizing, TDM starts in the maintenance mode for the beginning of the run and the up-down counter is set to its maximum value. A TDM test run is initiated by typing the $BITE command.

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```
$TDM
TDM IN?
Y
WHICH RECEIVER? A/B?
A
ENTER TDM FRAMING PATTERN, Z4 FORMAT
ABCD
ENTER TDM COUNTER SIZE
16
ENTER MAINTENANCE MODE ERROR LIMIT
0
ENTER SEARCH MODE ERROR LIMIT
0
ENTER SUPER FRAME PERIOD LENGTH
408
ENTER DOWN COUNT INCREMENT
1
<INDEXH>
```

Figure 5-22   TDM INITIALIZATION SEQUENCE

5.3.2 MAINTENANCE MODE

In normal circumstances, the maintenance mode of TDM is used. The maintenance mode is only left upon a loss of sync indication from the up-down counter. The following discussion explains the flow diagram of Figure 5-23, the maintenance mode algorithm.

When the period counter reaches 16, i.e., when the first 16 bits of the super frame are counted, frame sync is checked. These 16 bits, defined as the frame sync word, are compared to the framing pattern to check for correlation. If the number of discrepancies is greater than the number of errors acceptable for the maintenance mode, then no correlation is assumed and the up-down counter is decremented by a selected value. If the counter is decremented to zero, loss of sync is assumed. To verify a true or false loss of sync, the period counter is compared to the automatic frame counter. If they are the same, a false loss of sync is recorded. If they are different, a true loss of sync is recorded. The search mode is then entered for sync acquisition.

72
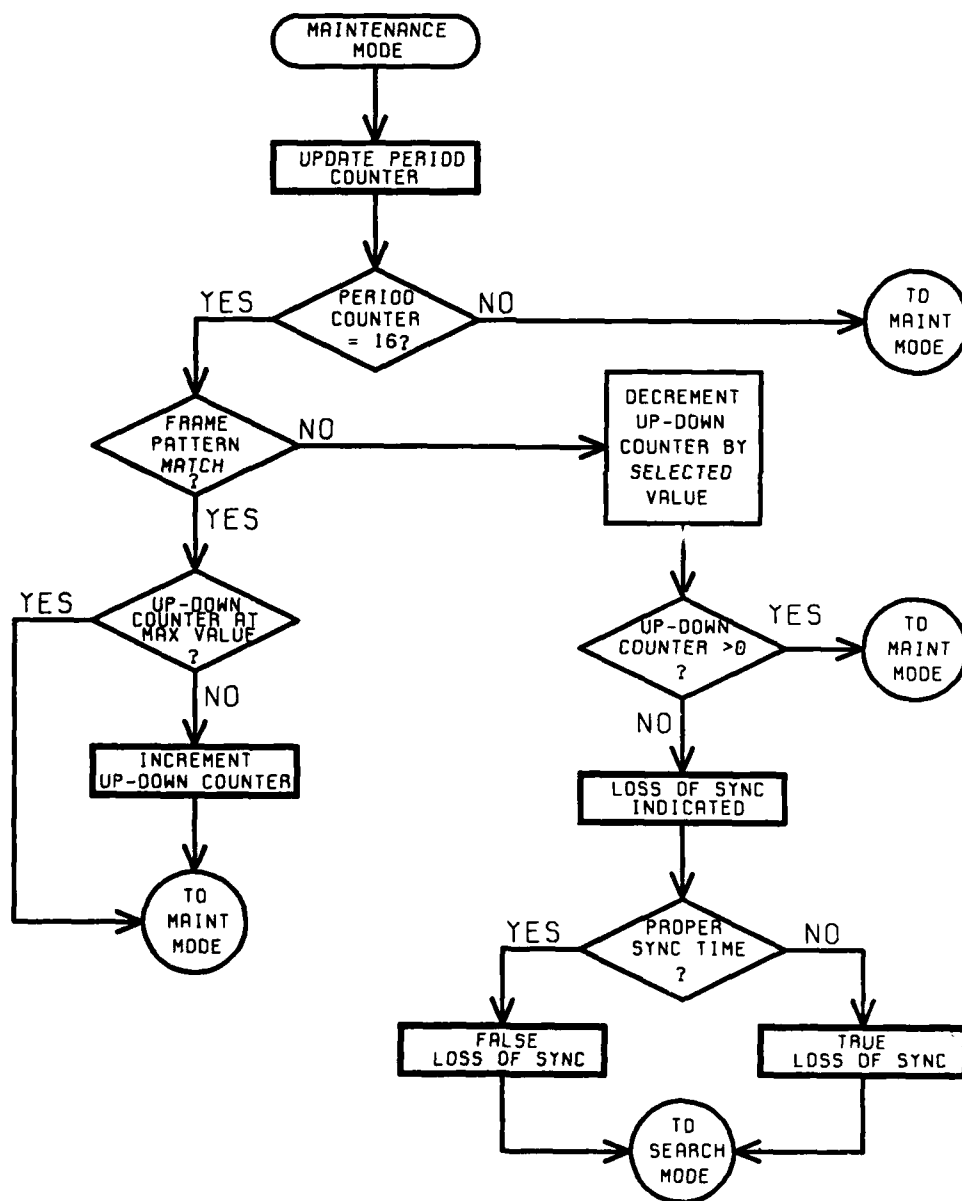
Figure 5-23   TDM MAINTENANCE MODE ALGORITHM

If the period counter is not equal to 16 as mentioned above, frame sync check time has not been reached. The period counter is then checked to see if the end of the super frame period has been reached. If so, the period counter is reset to zero. Control is then returned to the top of the loop for checking the next bit.

5.3.3 SEARCH MODE

If the up-down counter is decremented to the zero state due to poor correlation in the frame sync word and the framing pattern, the search mode is entered. This can occur due to a true loss of synchronization or a false loss of synchronization due to channel induced errors. Pertinent information is stored out about the loss of sync indication in either case.

The following discussion explains the steps in the flow diagram of Figure 5-24, the search mode algorithm.

Upon entry into the search loop, the first bit received is read from the receiver and the last 16 bits received buffer is updated. These 16 bits are then compared to the framing pattern to check for correlation. If the number of discrepancies is greater than the number of errors acceptable for the search mode, the loop is restarted and the next candidate, or bit, position is tried. This repeats until the number of discrepancies in a candidate position is less than or equal to the number of errors acceptable in the search mode. When this occurs, it is assumed that the proper frame location has been found and the search is complete. The up-down counter is then set to its maximum value and the period counter is reset to 16.

At this time, a check to see if the acquisition of sync was true or false is performed. This is done by checking to see if the automatic frame counter, which is always correct, is 16. If it is 16, a true acquisition of sync is recorded. Otherwise, a false acquisition of sync is recorded and control is transferred back to the maintenance mode.

5.3.4 OUTPUT MODE

Statistical averaging of time to true loss of synchronization, time to false loss of synchronization, and sync acquisition time are computed at the end of each TDM test. The user receives at the remote terminal a list of statistics summarizing the results of the user specified input data. A sample output summarizing the results of a TDM test is shown in Figure 5-25.
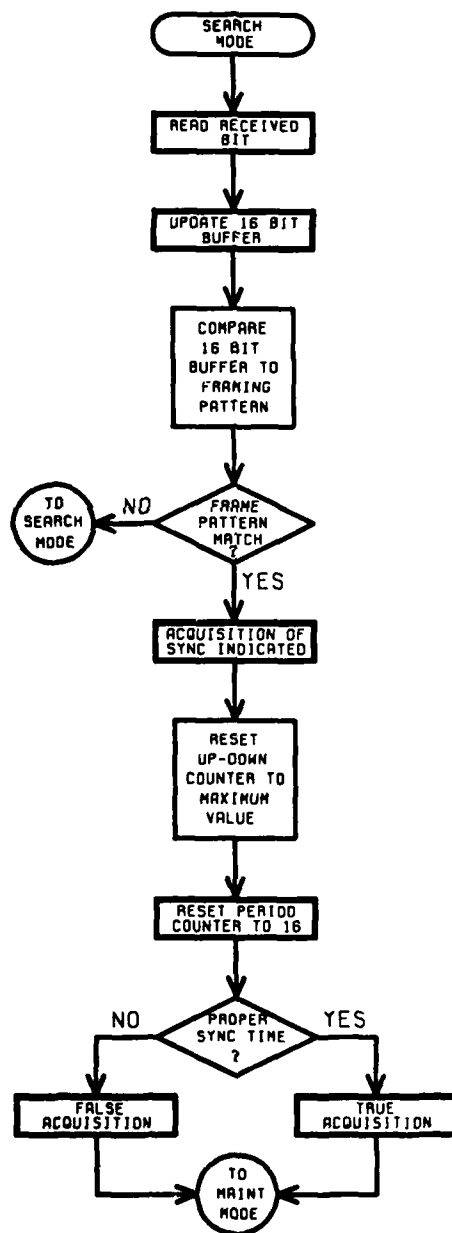
Figure 5-24   SEARCH MODE ALGORITHM

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```
TDM RESULTS:
NUMBER OF TRUE OR FALSE LOSSES OF SYNC.                                    9
NUMBER OF TRUE LOSSES OF SYNC.                                            6
NUMBER OF FALSE LOSSES OF SYNC.                                           3
NUMBER OF TRUE ACQUISITIONS OF SYNC.                                      3
NUMBER OF FALSE ACQUISITIONS OF SYNC.                                     6
MEAN TIME BETWEEN FALSE ACQUISITIONS OF SYNC.                66666 BITS
MEAN TIME FROM TRUE ACQUISITION TO LOSS OF SYNC.             78387 BITS
MEAN TIME FROM TRUE ACQUISITION TO FALSE LOSS OF SYNC.       78387 BITS
NUMBER OF TRUE ACQUISITIONS DUE TO TRUE LOSSES OF SYNC.                   3
MEAN TIME FROM TRUE LOSS OF SYNC TO TRUE ACQUISITION           108 BITS
NUMBER OF TRUE ACQUISITIONS DUE TO FALSE LOSSES OF SYNC.                  3
MEAN TIME FROM FALSE LOSS OF SYNC TO TRUE ACQUISITION         2040 BITS
NUMBER OF TRUE ACQUISITIONS DUE TO LOSSES OF SYNC.                        3
MEAN TIME FROM LOSS OF SYNC TO TRUE ACQUISITION              2040 BITS
NUMBER OF REJECTIONS OF FALSE SYNC.                                       6
MEAN TIME TO REJECTION OF FALSE SYNC.                          816 BITS
NUMBER OF TRUE SYNCS DUE TO FALSE SYNCS.                                  3
MEAN TIME FROM FALSE SYNC TO TRUE SYNC.                       1891 BITS
<INDEXH>
```

Figure 5-25   STATISTICS SUMMARY FOR TDM RUN

5.3.5 TDMINT SYNC ACQUISITION

TDM used in conjunction with TDMINT, is an analysis of the average time from start-up to true sync acquisition. In this mode, the primary function is the statistical averaging of true sync acquisition time.

Normally preceded by TDM initialization, TDMINT initialization and run mode is entered by typing the $TDMINT command. The user is prompted to input the number of runs to be averaged and the signal-to-noise ratio (EB/NO) for receivers A and B as shown in Figure 5-26.

For each run requested, TDM starts out in the search mode. Although false sync acquisitions may occur, individual runs are terminated only in response to a true sync acquisition. A "BEEP" from the user console signals true sync acquisition has been attained for that run in the sequence.

```
$TDMINT
HOW MANY RUNS TO BE AVERAGED?
20
ENTER EB/NO FOR CHANNEL A
9.0
ENTER EB/NO FOR CHANNEL B
9.0
<INDEXH>
```

Figure 5-26   TDMINT INITIALIZATION SEQUENCE

At the end of the runs, TDMINT initialization results are output to the user terminal. The statistical summary consists of the average acquisition time and variance for true acquisition, and the average acquisition time and variance for true and false acquisitions combined. A built-in time limit is imposed on TDMINT runs which means all runs may not be averaged if some runs reach the time limit before true sync acquisition is achieved. A sample output summarizing the results of a TDM test utilizing TDMINT is shown in Figure 5-27 .

```
TDM INITIALIZATION RESULTS:
    20 RUNS AVERAGED
     0 RUNS TIME LIMIT REACHED
FRAME LENGTH =          408 BITS

TRUE AQUISITION:
AVG. ACQ. TIME=    1084.0 BITS
VARIANCE       = 0.152E+07 BITS

TRUE/FALSE AQUISITION:
AVG. ACQ. TIME=    1084.0 BITS
VARIANCE       = 0.152E+07 BITS

<INDEXH>
```

Figure 5-27   STATISTICS SUMMARY FOR TDMINT TEST

5.4 RECEIVED SIGNAL LEVEL MONITOR

The Received Signal Level Monitor is used to control the diversity switch and may be combined with other monitors to determine switch position. The receiver IF amplifiers are each supplied gain control multipliers at their inputs. These multipliers are driven by amplified analog signals derived from the filtered output of the AGC circuit. Using the output of this filter to drive a log function preloaded in the MFTP, a linear indicator of the received signal level (RSL) in dB is generated.

This linearity has been tested and is linear within +1 dB. The RSL monitor bandwidth may be varied from 0.001 Hz to 10 Hz by the simulation user.

When using RSL as the diversity driving function, the difference between RSLA and RSLB is tested. If the absolute value of this difference is greater than an operator chosen threshold (Th2), then the receiver with the greater signal level is chosen. If the difference is less than Th2, no change in switch position is made. Th2 is nominally set at 6 dB.

5.5 IMPROVED SIGNAL QUALITY MONITOR

The improved signal quality monitor is composed of two subsystems. They are the offset threshold monitor and the pseudo error counter.

The offset threshold monitor compares the baseband signal pulse amplitudes to user set acceptance ranges that are a percentage of the peak signal level. If the pulse amplitude at the time of sampling is outside of the acceptable range, then a pseudo error pulse is generated. This is shown in Figure 5-28.

α, which defines the pseudo error band, is determined by the simulation user. The Offset Threshold Monitor (OTM) user option requests the desired α from the user. This program calculates and changes the threshold levels to match the user selected α.

Threshold levels are calculated as follows:

The α given by the user is a percentage of peak pulse amplitude.

This percentage is the width of an error band centered around one half of the peak value. The remaining percentage of peak amplitude is K, where K=1.0 - α. The lower threshold value is Peak multiplied by K/2. The upper threshold Peak is multiplied by (1.0 - K/2). This is shown in Figure 5-28.

The hybrid circuitry for the offset threshold monitor is composed of comparators and logic as shown in Figure 5-29.

Inputs to the improved signal quality monitor are the A channel and B channel pseudo errors generated by the OTM. The diversity decision is based on the output of a digitally programmed up/down counter. Nominally, the counter is initially loaded with one half of this maximum count. The counter then counts up on each A channel pseudo error and counts down on each B channel pseudo error. If the counter underflows, the diversity switch is set to A channel, an overflow causes the switch to change to B channel. This is shown in Figure 5-30.

The current counter size of the monitor is now 14 bits. A user option is available to initialize the counter to any size with 7 bits being nominal. A diversity decision flow chart is given in Figure 5-31. A hysteresis run option is now available. The user initializes the counter and receiver selection and then starts a run, which is terminated upon diversity switch. A sequence of runs can be made in this fashion with run averages made available at the end of the series.
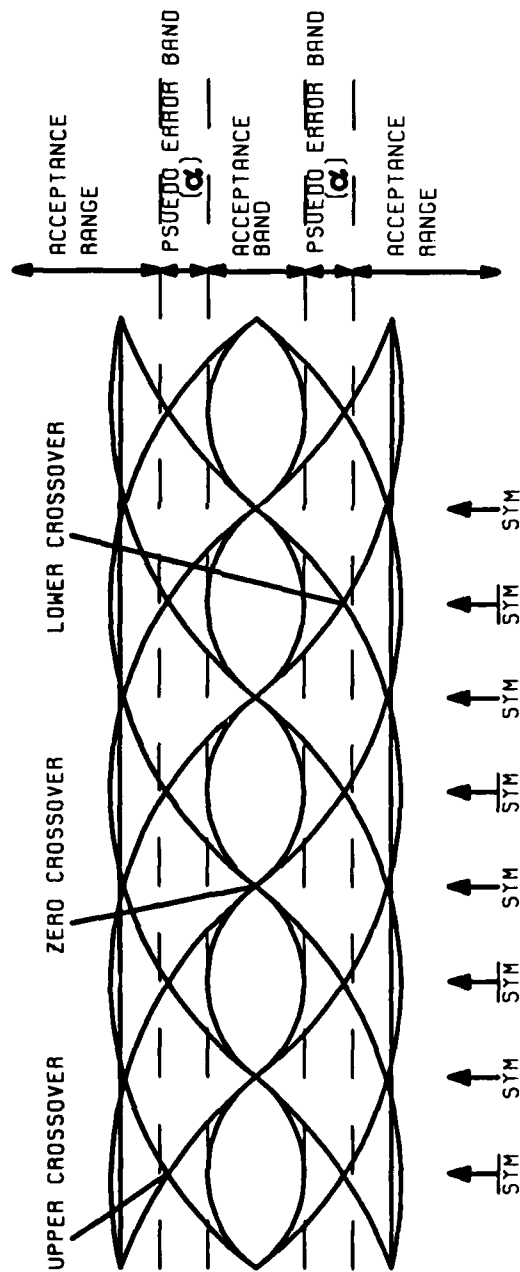
Figure 5-28   BASEBAND THRESHOLD LEVELS
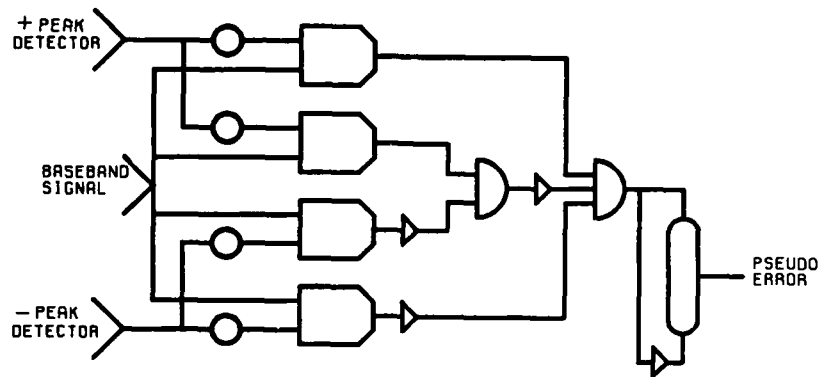
Figure 5-29   OFFSET THRESHOLD MONITOR SIMULATION
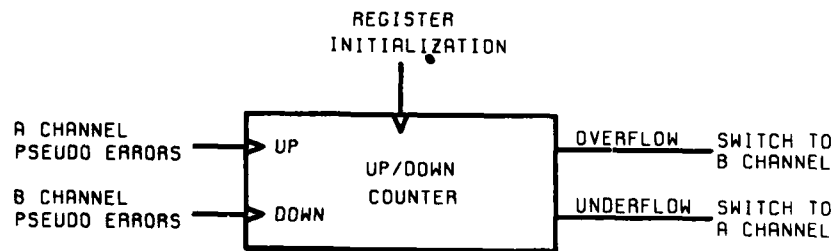
Figure 5-30   PSEUDO ERROR IMPROVED SIGNAL QUALITY MONITOR

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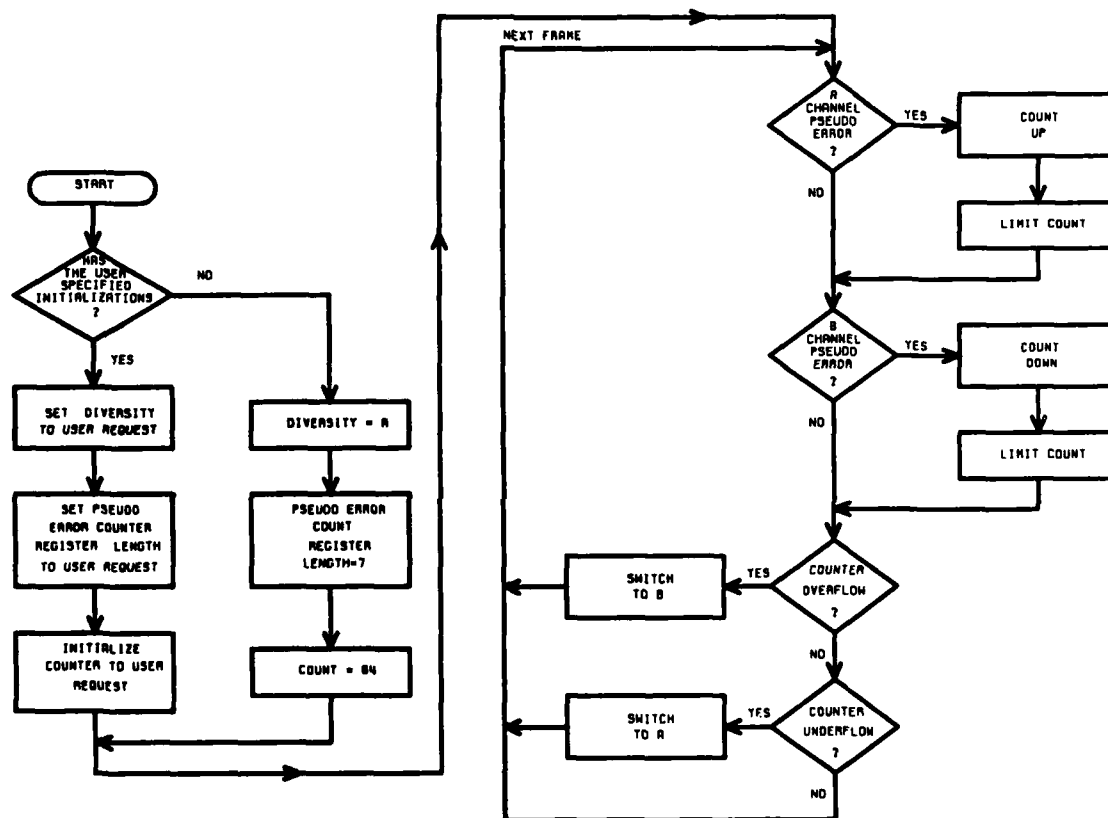
Figure 5-31   ISQM DIVERSITY ALGORITHM

5.6 IMPROVED DUAL DIVERSITY SELECTION COMBINER

In the improved diversity selection algorithm two performance monitors are available as diversity driving functions. The available driving functions are received signal level (RSL) and improved signal quality monitor (SQM). Both driving function options are available in conjunction with all other simulation options.

Selection of the driving function is made by the simulation operator. Decisions made by the algorithm are dependant upon choices of threshold values also made by the operator.

The algorithm for the improved dual diversity selection is given in Figure 5-32.
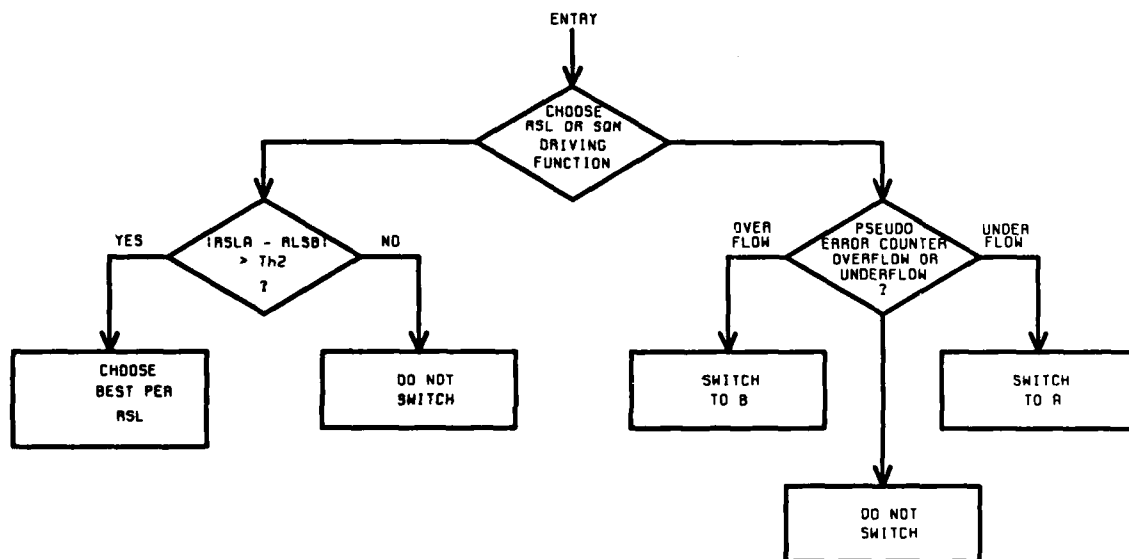
Figure 5-32 DIVERSITY COMBINER ALGORITHM

5.7 FADE OUTAGE MONITOR

The fade outage monitor gives an indication of percent time each receiver's signal level spends below an optional bit error rate threshold level. This threshold is selectable by the simulation user. An analog circuit measures IF signal strength in dB at each receiver. A data comparator is then used to compare the signal strength level with an adjustable fade outage threshold level for both receivers. The data comparators are then monitored each frame by the digital computer. A counter is incremented, for each receiver, each time the data comparator indicates the signal strength is below the fade outage threshold level. A third counter is also incremented every frame for a time count. Upon termination of the simulated run, the percent fade outage for each receiver is computed by dividing each receiver counter value by the time counter value and multiplying by 100. Figure 5-33 shows the analog block diagram and digital flowchart for this implementation.
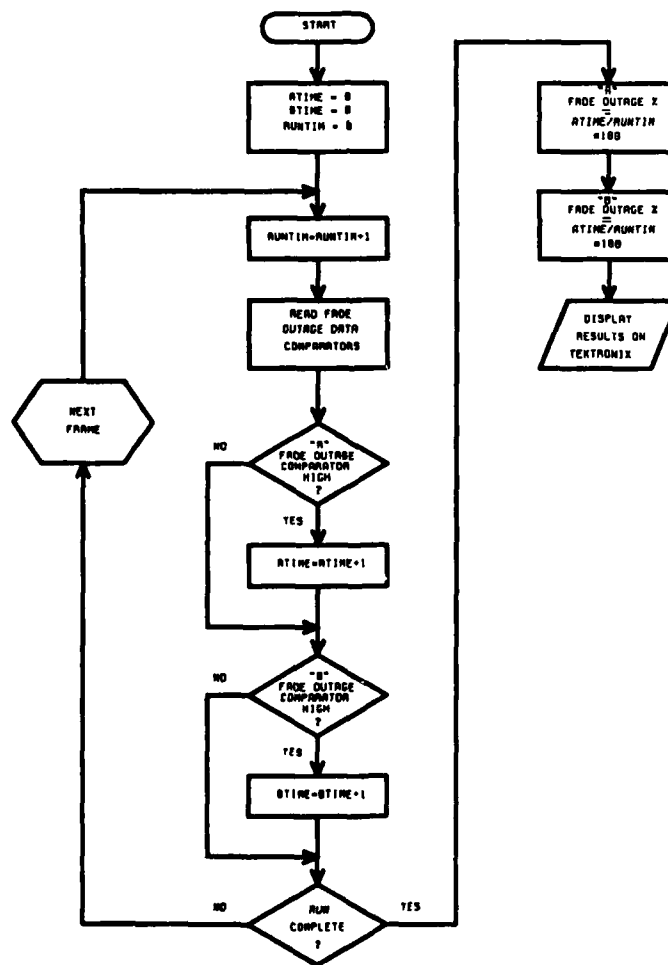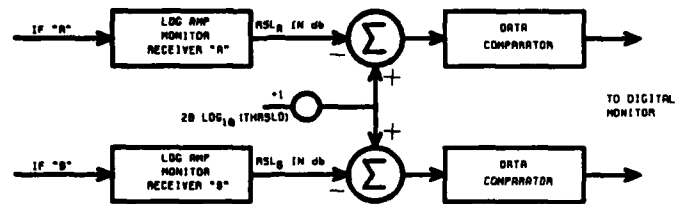
Figure 5-33   FADE OUTAGE MONITOR SIMULATION

6. LOS CHANNEL MODEL

This section describes the present channel model for use with the AN/FRC-170(V) radio hybrid simulation and the modteq simulation..

6.1 FREQUENCY SELECTIVE FADING MODEL

The LOS simulator is made up of three elements: a delay line module, a digital filter module, and a multiplier-summer module. The simulation model allows the user to change the tap gains, tap delay spacing, and signal-to-noise ratio. Figure 6-1 provides an overall block diagram of the channel model. The LOS channel model digital program allows the simulation user to specify the number of taps desired (from 1 to 12).

The delay line is a general purpose channel model which was built during the 12 month FY-83 contractual period. It is composed of a 12 bit 2 microsecond analog to digital converter, a 48 kiloword, (each word being 12 bits wide) RAM, and twenty four 12 bit digital to analog converters. The 12 bit accuracy yields a 72 dB signal to noise ratio throughout the system.

The 24 D/A's can be divided into 12 pairs of 2. Each pair consists of a co-phasal and quadrature output couple for simulating the dynamically fading path situation.

The 12 delay line pairs are actually 12 stages in a serially cascaded 12 stage delay line. The output of pair "N" is the output of pair "N-1" delayed in time by τ microseconds. τ may range from 2 to 8192 in steps of 2. This corresponds to 0.002 to 8.192 bit intervals of inter-tap spacing, satisfying the 0.025 to 2.5 bit interval requirements stated in the statement of work. A block diagram of the cascaded delay line section is shown in Figure 6-2.

The digital filter module has been implemented on the hybrid computer system's digital computer. The digital computer provides the resources to generate 48 uncorrelated random noise sequences, filter them, and transfer the resulting signals to the multiplier summer module. The 48 random noise sequences were generated by sampling a Gaussian pseudo-random number generator. Capability exists to provide correlation between adjacent random noise sequences by numerically combining two independent noise sources in a controlled process. The digital filters are second order Butterworth types, with nominal cutoff frequency equal to the fade rate, with a calculated optimal sampling frequency up to 83 samples per second. The cutoff frequency can be selected by the remote hybrid terminal user at DCEC with a range between 0 and 2000.0 time scaled hertz. The 48 Gaussian noise output signals from the digital filter are multiplied by the mean power coefficient at that tap, and then input to the multiplying digital-to-analog converters (MDAC) in the multiplier-summer module.
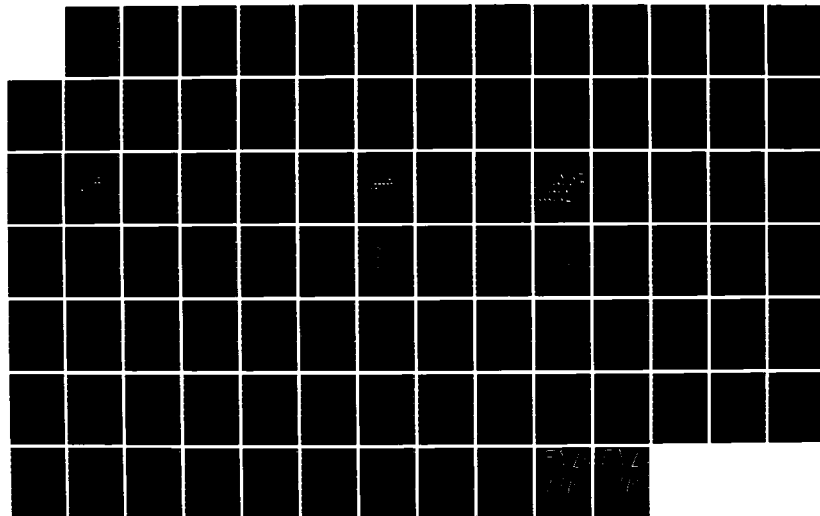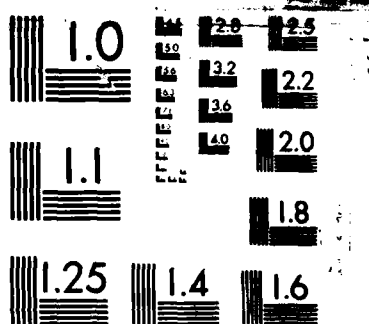
MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS
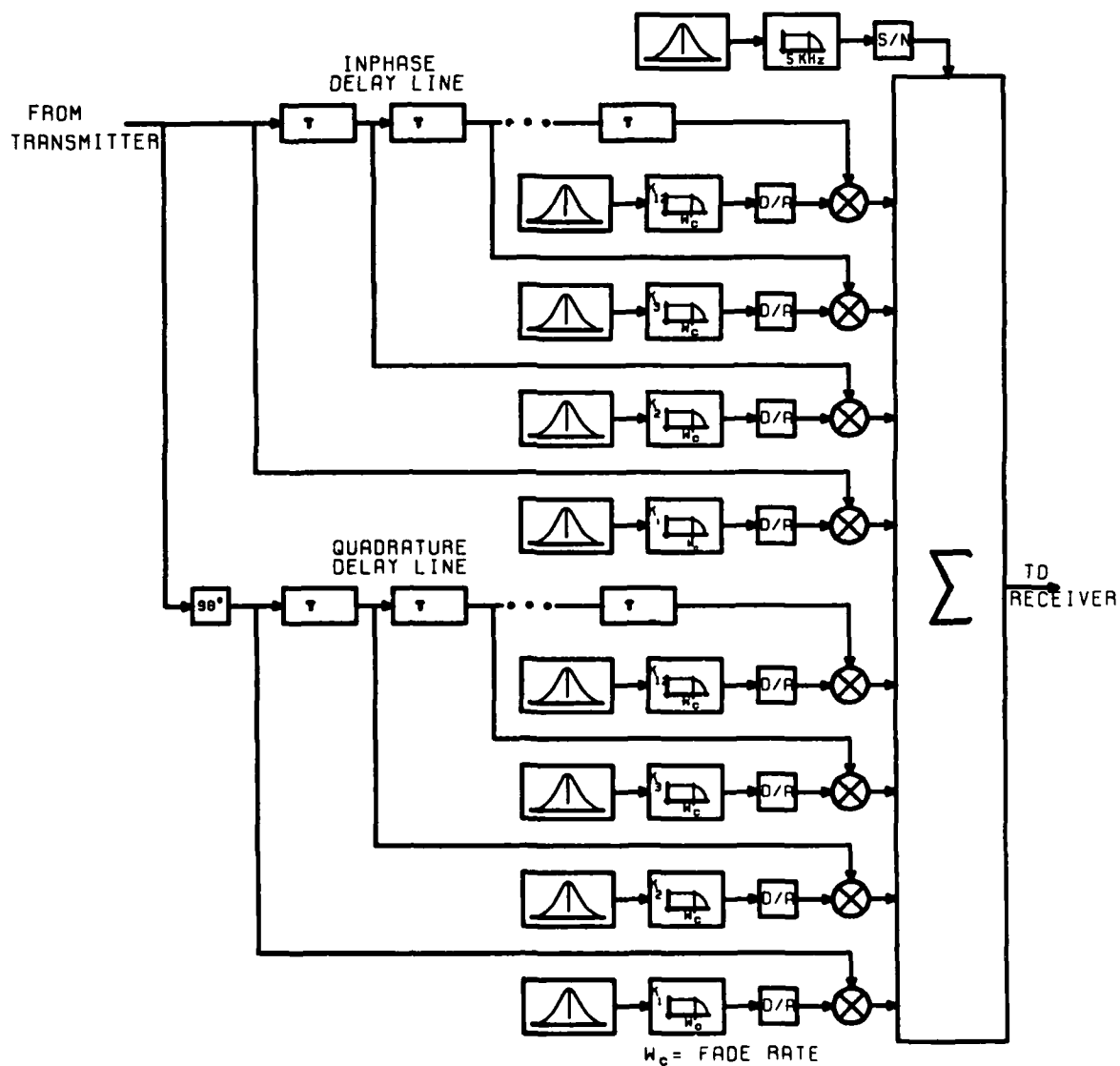
Figure 6-1   LOS CHANNEL MODEL
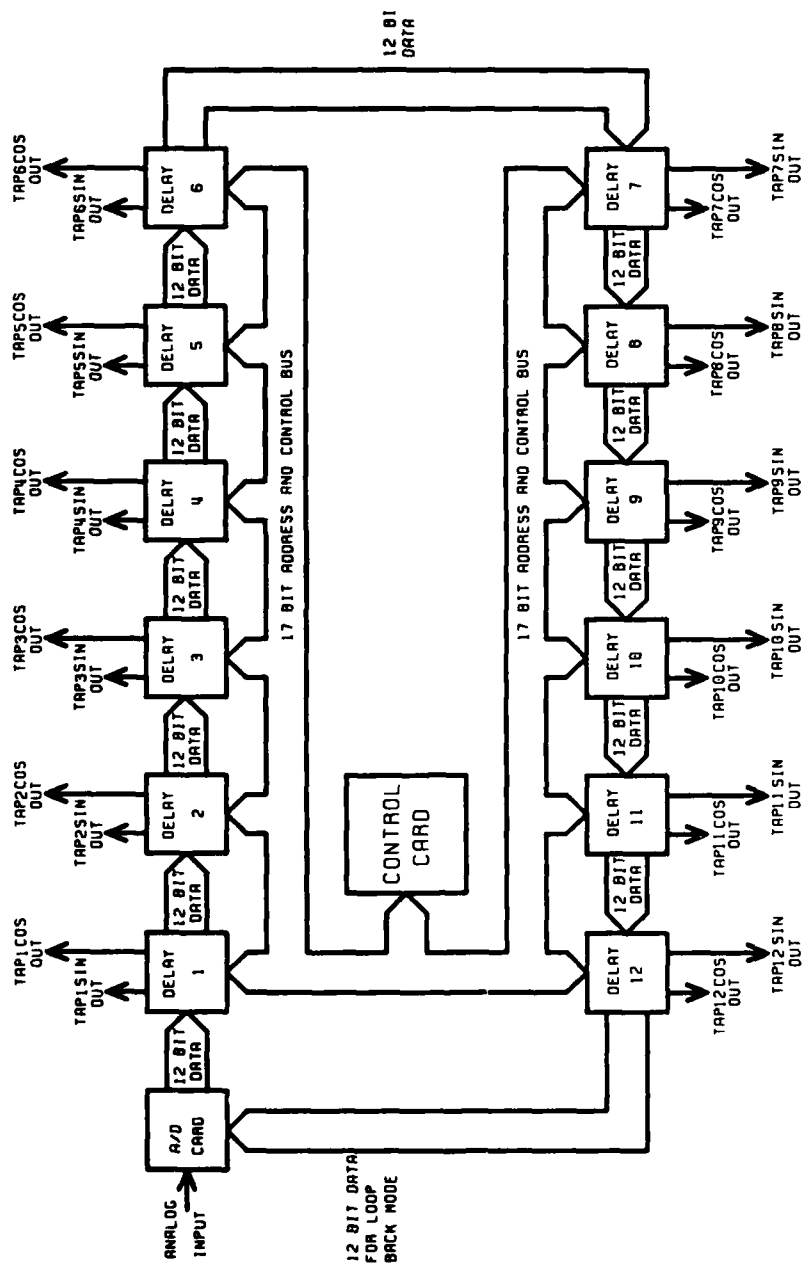
Figure 6-2 BLOCK DIAGRAM OF DELAY LINE

The multiplier-summer module for LOS consists of 2 channels, each of which contains 12 pairs of MDACs (1 pair per delay line tap) and a summing amplifier. One power coefficient in each pair multiplies the signal from one of the taps in delay line 1 by one of the Gaussian functions, $G_i(t)$, while the other power coefficient multiplies the signal from the corresponding tap of delay line 2 (which is delayed an additional $\pi/2$ radians) by another Gaussian function, $G_j(t)$. The output of the 12 MDAC pairs is then summed by an analog summing amplifier network to provide the final channel output.

Additional enhancements made to the channel model are separately controllable signal-to-noise ratios and tap gains for each channel, selectable stationary or Rayleigh fading taps for each receiver, increased tap width of 0.002 to 8.2 bit widths, and remote display, with hardcopy, of each channel model configuration. Individual adjustment of tap fade rates from 0 to 1 Hz are also possible.

7. NAKAGAMI-RICE FADING CHANNEL

This section contains a description of the work performed in accordance with task 2 of statement of work R220-85-011. Task 2 requests the addition of a Nakagami-Rice fading characteristic which can be applied to the general purpose channel model. The research, implementation, and verification of this work was performed using FY-85 funds. Figure 7-1 is a block diagram of the implementation.

The Nakagami-Rice channel model is similar to the Rayleigh fading channel model in that the resultant signal can be modeled mathematically as the sum of two independantly fading quadrature components. The Rayleigh characteristic is actually a subset of the Nakagami-Rice characteristic. The difference is that the Nakagami-Rice channel also contains a non-fading component. The non-fading component can be in phase reference to the zero degree term, ninety degree term, or any constant phase combination. If the amplitude of the non-fading component is set to zero, the result would be a Rayleigh fading characteristic. This Rayleigh characteristic is because each of the quadrature amplitude profiles is Gaussian, as in Rayleigh.

Of paramount importance to the Nakagami-Rice characteristic is the control parameter referred to as the 'Multipath Occurrence Factor'. The letter 'd' is commonly used to represent the multipath occurrence factor in mathematical expressions. The multipath occurrence factor controls the relative strengths of the Rayleigh component and the constant amplitude term. Actually, the RMS value of the Rayleigh amplitude profile is used since the instantaneous amplitude is constantly changing. Letting 'N' represent the constant term amplitude, and letting 'R' represent the composite Rayleigh RMS amplitude, the ratio N/R is calculated as follows based on 'd', the multipath occurrence factor:

$$N/R = SQRT[-\ln(d)]$$

It was stated earlier that the Rayleigh fading characteristic is a subset of the more general Nakagami-Rice characteristic. This case is realized by letting 'd' go to unity. This is expected since a purely Rayleigh characteristic is representative of a randomly fading channel, (unity multipath occurence factor). In this case, 'N', the constant amplitude gain, would be zero. A non-fading characteristic is achieved by letting the RMS Rayleigh amplitude ('R' in the above equation) go to zero. In this case 'd' would go to zero as well, and hence, a zero multipath occurrence factor.
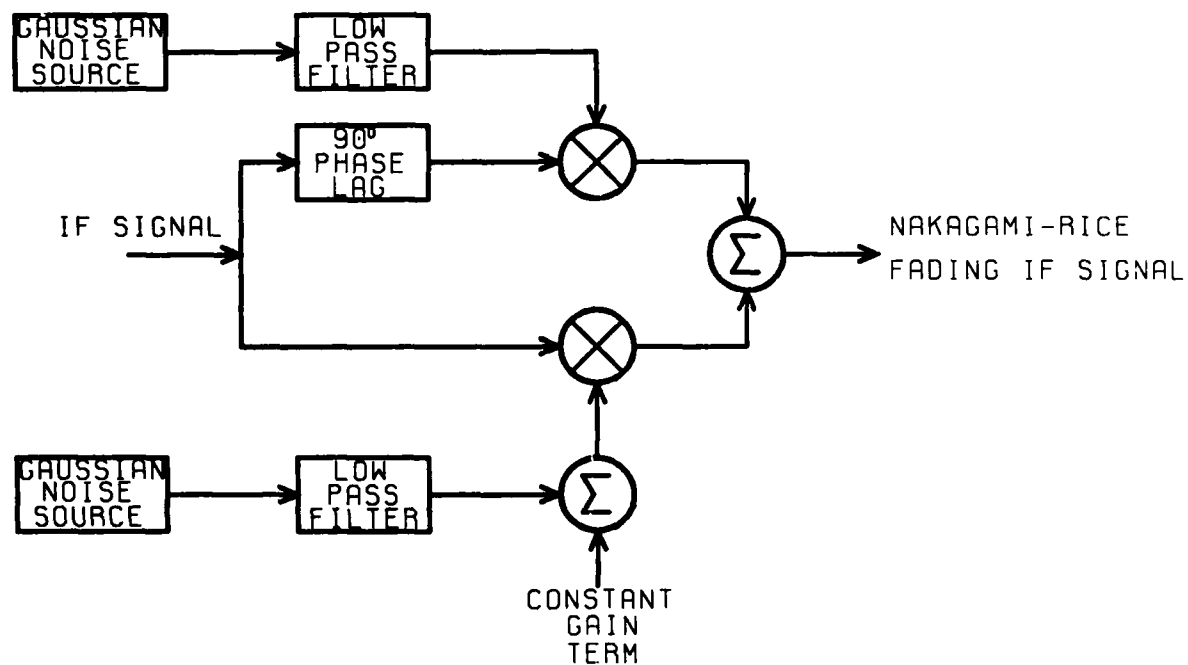
Figure 7-1   NAKAGAMI-RICE BLOCK DIAGRAM

8. HARDWARE AND SOFTWARE SUPPORT

This section describes the hardware and software support provided to DCEC as described in Tasks #4 of statement of work R220-85-011/Jan. 85. Funds for these tasks are allocated in FY-85.

8.1 AN OVERVIEW

A significant part of the AN/FRC-170(V) hybrid radio simulation is the host digital computer. The digital computer used for this contract is a Gould model 32/27. The 32/27 is a 32 bit scientific machine with a 100 nanosecond cycle time.

Some of the tasks the machine will perform for the DRAMA and MODTEQ projects are, system set-up system verification, system modification, system monitoring, improved signal quality monitor activities, remote user interfacing, Ptran, Fortran and assembly language program modification and overall system integration.

Section 8.6 discusses the analog stripplot capabilities.

Figure 8-5 displays how the digital interfaces with the simulation and remote user.

8.2 THE USER'S PROGRAM

The DRAMA digital program currently consists of approximately 12,000 lines of Fortran VII and assembly language. The MODTEQ digital program is simplistic, but is being progressively expanded to incorporate additions to the simulations on the Simstar system. The Modteq software is included as Apendix A. The Fortran is used in non-real time applications to allow for ease of modification. The assembly language code is used in the real time applications such as bit error testing, and random number generation

In DRAMA, all of the hybrid interface functions can be commanded either through Fortran calls or assembly language calls for high speed execution. Both methods are used in the user's program. In Modteq, the hybrid calls are performed by a separate processor invoked by either the Simstar parallel processor or through Fortran calls.

The programs allow either local or remote operation.

8.3 HYBRID COMPUTER REMOTE TERMINAL PROVISION

Martin Marietta Technical Computing Center maintains the capability to provide the Defense Communications Engineering Center (DCEC), Reston, Virginia, with an advanced hybrid computer terminal through which they are able to operate and control the hybrid computer simulations developed in this study.

This terminal uses two telephone lines and the equipment listed below to provide stripchart analog recordings for eight channels, digital graphical displays, and control of the hybrid simulation at Orlando, Florida. The terminal equipment loaned to DCEC consists of the following items:

o 1 One Tektronix 4010 Terminal

o 2 One Tektronix 4620 Hard Copy Unit

o 3 One EMR Remote Terminal

o 4 One Eight-Channel Brush Recorder

o 5 One Universal Data Systems EC212A/D Error Corrective Full Duplex Telephone Modem

o 6 Two 1000a Data Couplers

The two telephone 1000A Data Couplers supplied by Martin Marietta Aerospace and installed at the DCEC facility at Reston, Virginia, are required as part of this installation to permit interchange of hybrid computer data with Orlando, Florida. The EC212A/D modems were purchased to eliminate problems associated with the noisey long distance lines used to connect the remote user to the TCC lab. the new modems use error corrective processing to alleviate the bit errors generated over the phhone lines. The Tektronix Terminal and hardcopy units allow the customer to control the simulations and obtain results, both tabular and graphic by use of the commands described in Section 8.4 and 8.5.

Figure 8-5 depicts the overall layout of the system.

8.4 USER DISPLAYS AND CONTROLS

The simulation software for the hybrid simulation evaluation of frequency selective fading of DCS digital LOS radio equipment is a set of digital programs and subprograms that allow the remote terminal user to interface with the Martin Marietta hybrid computer simulation system by means of the remote terminal at DCEC. This versatile group of programs permits the remote terminal user to alter the system configuration, change system parameters, test and verify system elements, and yield sufficient data to make analytical evaluation of transmission system performance.

INDEXH, the program monitor, gives the remote terminal user the full flexibility of the hybrid programmer operator. Requests to INDEXH provide access to all the program options. The majority of those are under the digital computer's control, hence are automatically integrated into the system. Some options require intervention by the hybrid operator and the remote user is requested to wait.

For DRAMA, input to INDEXH is through the Tektronix graphic input terminal, and the output of the system simulation is to that terminal in the form of graphic and tabular data, and to the eight-channel stripchart recorder. The problem variables are all available for output to the eight-channel stripchart recorder. Two preset variable lists can be arranged at the time of operation such that the user may select either set. Other variables may be selected at any time to replace one or more of those in the preset lists. This is an example of a system change requiring operator intervention. Figure 8-6 is a partial alphabetical list of commands recognized by INDEXH.

For MODTEQ, command input is supplied via a menu driven piece of software written specifically for MODTEQ. Additional commands of MODTEQ include modulation technique and level selection, and baseband filter rolloff modification. Examples of use of the menu driven software are provided in Section 8. Commands will be added to accommodate additions to the simulation as they are developed.

8.4.1 ADDED USER SOFTWARE

For DRAMA, two new commands have been added for monitoring the performance of the baseband equalizer. These are described in Section 8.4.1.1.

For MODTEQ, a menu-driven user software package is available to change parameters between runs. Conditions of the radio which can be changed include the number of bits per symbol and the bandpass filter models in the transmitter and receiver. The software is set up to handle changes in the environment such as EB/NO and multipathing.

User software prompts during a typical simulation setup are shown. User input is shown in *italics*. The computer prompts are shown in **bold**.

START
    WHAT DO YOU WISH TO DO?
    1 START RUN
    2 SPECIFY NEW RUN CONDITIONS

    >*2*
    WHAT DO YOU WANT TO CHANGE?
    1 TRANSMITTER / RECEIVER
    2 ENVIRONMENT

```
>1
WHAT DO YOU WANT TO CHANGE?
1 BANDPASS FILTER MODELS
2 BITS PER SYMBOL

>2
ENTER 1,2, OR 3 BITS PER SYMBOL

>2
WHAT DO YOU WISH TO DO?
1 START RUN
2 SPECIFY NEW RUN CONDITIONS

>1

*PROGRAM EXECUTING*
```

The following prompts show the flexibility of parameter changes in the bandpass filter model and the frequency response plot option.

```
CHANGE THE BANDPASS FILTER IN THE:
1 TRANSMITTER
2 RECEIVER
3 BOTH TRANSMITTER AND RECEIVER

>1
ENTER TRANSMIT FILTER TYPE
1 CHEBYCHEV
2 BUTTERWORTH
3 BESSEL

>2
ENTER CENTER FREQUENCY AND BANDWIDTH IN Mhz >  70,40
DO YOU WANT A FREQUENCY RESPONSE PLOT ? (Y or N) >  Y
ENTER BEGINNING AND END FREQUENCIES IN Mhz >  30,200
INPUT NUMBER OF PLOT POINTS (MAX=200) >  200
```

The frequency response output of the program is depicted in Figure 8-1.
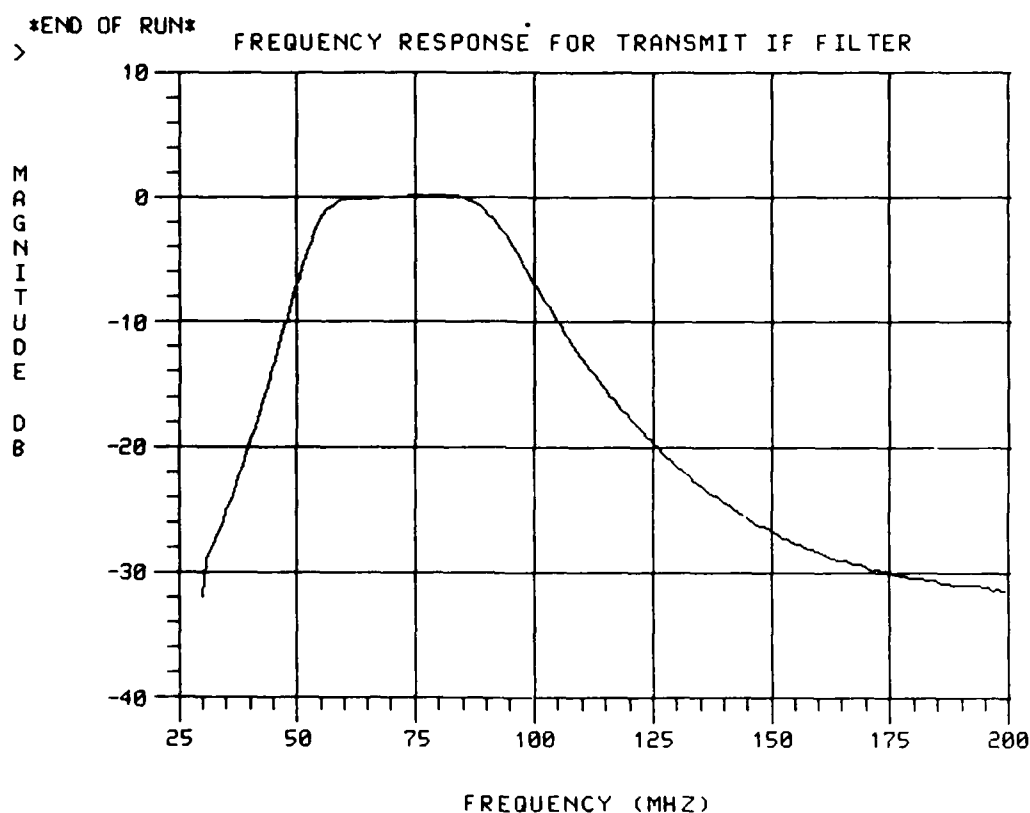
Figure 8-1 FREQUENCY RESPONSE

8.4.1.1 NEW DRAMA COMMANDS

Two new commands have been added to the complement of directives available to the DRAMA simulation user. These commands are '$CONST' and '$CONVRG'. The CONVRG command is used to obtain a point constellation of the quadrature baseband signals. The baseband signals used are taken from the outputs of the baseband equalizer. The user can then obtain visual results of the unequalized performance by using the '$BBE' command to turn off the effect of the FFE and DFE prior to using the $CONST command. An example of this output is shown with some channel multipathing incorporated in Figure 8-3. The user then uses the '$BBE' command to turn on both the FFE and DFE before again running the CONST routine to obtain a point constellation plot of the equalized quadrature baseband signals. An example

of this output is provided in Figure 8-2. A typical invocation of the CONST routine is shown below. User input is shown in *ITALICS*. Computer output is in **BOLD**.

$CONST
HOW MANY POINTS TO PLOT? **< 750**
200
ENTER GRAPH COMMENT
AN EXAMPLE OF A POINT CONSTELLATION

Inspection of Figures 8-3 and 8-2 reveal the improvement in data estimation reliability due to the effects of the FFE and DFE.

The '$CONVRG' command is used to show the time required for the baseband equalizer coefficients to conform to a step change in the multipathing characteristics of the channel model. A typical invocation of the routine is provided below.

$CONVRG
ENTER GRAPH COMMENT
A CONVERGENCE TIME EXAMPLE
ENTER DESIRED RUN TIME IN SECONDS
60

A typical output from the CONVRG routine is supplied in Figure 8-4.
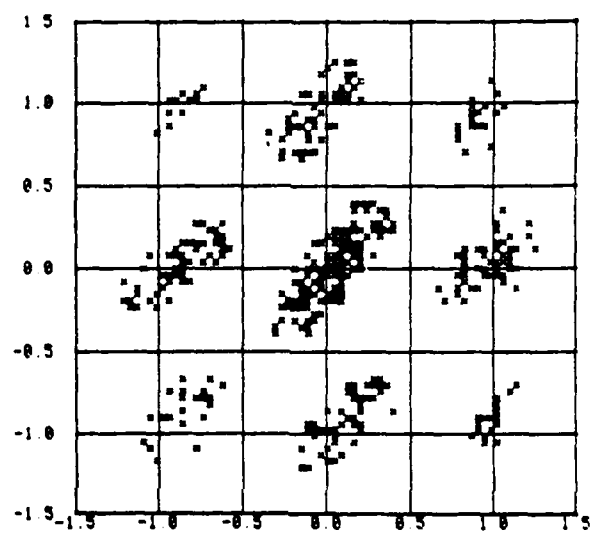
Figure 8-2   CONSTELLATION WITH FFE AND DFE BOTH TURNED ON
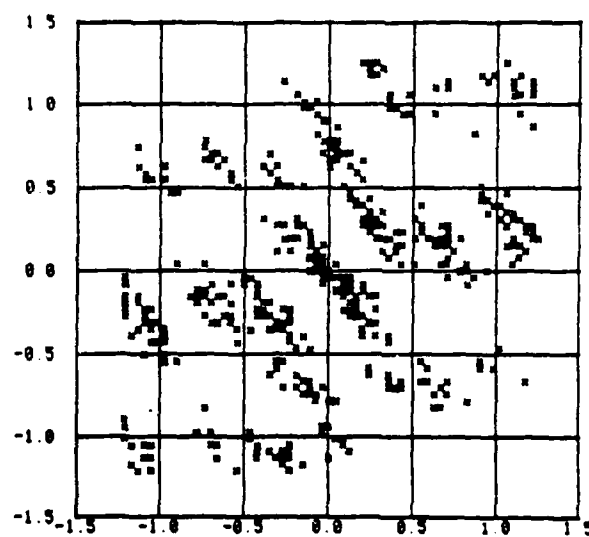
Figure 8-3 CONSTELLATION WITH FFE AND DFE BOTH TURNED OFF

A CONVERGENCE TIME EXAMPLE

AVERAGE EQUALIZER COEFFICIENT MAGNITUDE VS. TIME
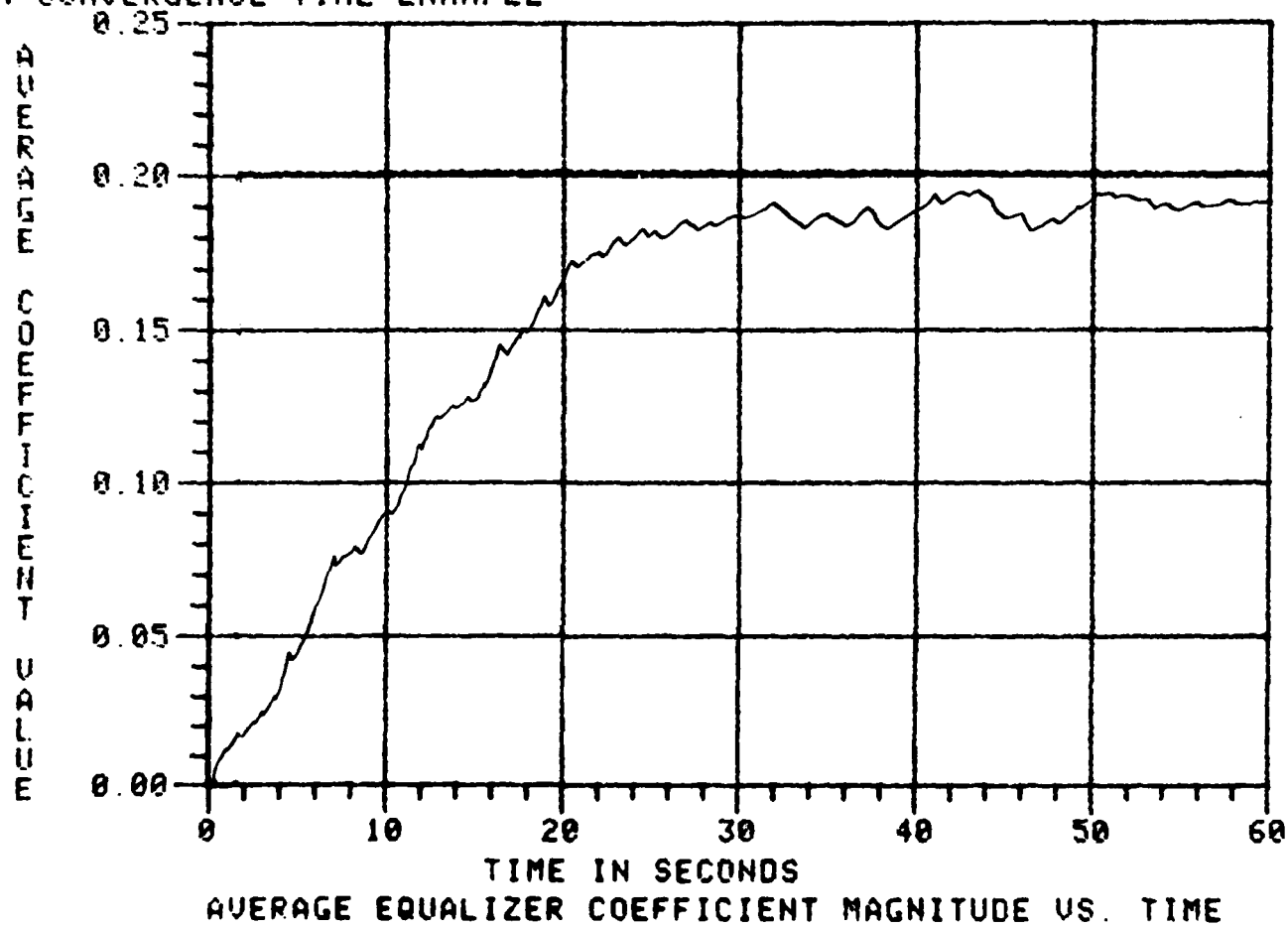
Figure 8-4   EXAMPLE OF CONVRG OUTPUT
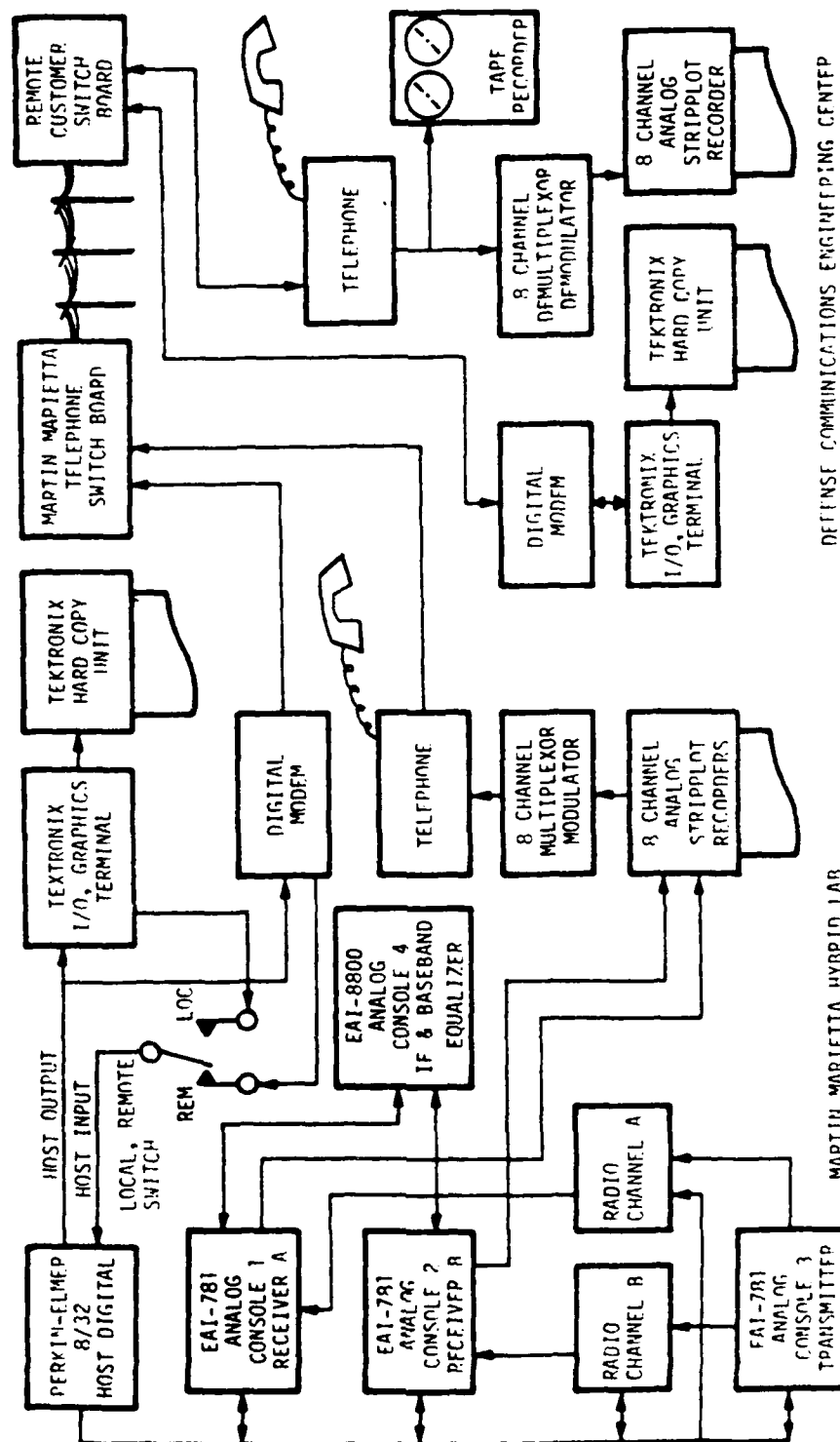
Figure 8-5 OVERALL SYSTEM LAYOUT

```
COMMAND
$AGC
$BBE
$BEEP
$BITE
$CHN
$CONST
$CONVRG
$CPY
$CRL
$CUR
$DPR
$DVR
$EBN
$EYE
$FOM
$FREQ
$FTEST
$HELP
$IFE
$IFEIN
$IFEOUT
$ITS
$LOCAL
$MODU
$NLI
$OTM
$PEC
$PGE
$PSD
$RSL
$RUN
$RUN5
$SCR
$SETUP
$TAP
$TDM
$TDMINT
$VIEW
```

Figure 8-6   INDEXH COMMANDS

8.5 USE OF COMMANDS

The following is a partial alphabetical grouping of commands and a brief explanation of their use. New commands will be added as required for support of the simulations.

8.5.1 $AGC COMMAND

Used for controlling whether the AGC is selected or deselected. Also controls the AGC cutoff frequency.

8.5.2 $BBE COMMAND

Used for setting options for Baseband Equalizer simulation.

8.5.3 $BEEP COMMAND

Used for bringing co-operator's attention to the terminal. Causes the bell to sound 5 times.

8.5.4 $BITE COMMAND

Used for invoking real time tests of the radio's bit error rate performance.

8.5.5 $CHN COMMAND

Used for selecting channel type, out, Rayleigh or line of sight.

8.5.6 $CONST COMMAND

Used for obtaining plot of point constellation.

8.5.7 $CONVRG COMMAND

Used to show time required for baseband equalizer coefficients to conform to a step change in the multipathing characteristics of the channel model.

8.5.8 $CPY COMMAND

Used for creating a hard copy of what is on the screen at both the local and remote site terminals.

8.5.9 $CRL COMMAND

Used for setting the correlation coefficient between random driving functions of the two channel models.

8.5.10 $CURVE COMMAND

Used to create graphs of bit error rate versus EB/N0, pseudo error rate versus EB/N0 and pseudo error rate versus bit error rate.

8.5.11 $DPR COMMAND

Used to select system drive power.

8.5.12 $DVR COMMAND

Used to select the diversity combiner technique, AGC or ISQM. The HYSTERESIS option is a run averaging technique for studying ISQM efficiently.

8.5.13 $EBN COMMAND

Used for setting the EB/N0 setting for idle time mode.

8.5.14 $EYE COMMAND

Used to display the present eye pattern of signal constellation for either receiver.

8.5.15 $FOM COMMAND

Used to select or deselect the activity of the fade outage monitor.

8.5.16 $FREQ COMMAND

Used to obtain a frequency response of any of the filters or channel models in the system.

8.5.17 $FTEST COMMAND

Used to get a set of all of the pertinent filters frequency responses.

8.5.18 $HELP COMMAND

Used for bringing co-operator's attention to terminal. Causes the bell to sound 5 times.

8.5.19 $IFE COMMAND

Used to select or deselect the IF Bump and Slope equalizer. If selected, the control parameters are input. Also the user may command a recalibration if desired.

8.5.20 $IFEIN COMMAND

Used after $IFE for selecting the IF equalizer without changing parameters.

8.5.21 $IFEOUT COMMAND

Used after $IFE or $IFEIN for deselecting the IF equalizer.

8.5.22 $ITS COMMAND

Used for selecting inter-tap spacing.

8.5.23 $LOCAL COMMAND

Used for optimizing graphics speed for local only running.

8.5.24 $MODU COMMAND

Used for selecting modulation type.

8.5.25 $NLI COMMAND

Used for selecting or deselecting the TWT non-linearity characteristics.

8.5.26 $OTM COMMAND

Used for setting the offset threshold monitor window width.

8.5.27 $PEC COMMAND

Used for setting the pseudo error counter register parameters.

8.5.28 $PGE COMMAND

Used to clear the screen on both the local and remote terminal.

8.5.29 $PSD COMMAND

Used to obtain a power spectral density of various signals throughout the system. The signals available to be accessed are:

- o a) Transmitter I Baseband output

- o b) Transmitter Q Baseband output

- o c) Transmitter RF filter #1 output

- o d) Transmitter TWT output

- o e) Transmitter RF filter #2 output

- o f) Channel A output

- o g) Channel B output

- o h) Transmitter modulator output

- o i) Receiver A, I Baseband output

- o j) Receiver A, Q Baseband output

- o k) Receiver B, I Baseband output

- o l) Receiver B, Q Baseband output

- o m) Utility input

8.5.30 $RSL COMMAND

Used to select or deselect the received signal level probability distribution function recording option for a $BITE run.

8.5.31 $RUN COMMAND

Used to initiate a $BITE run with the same run time parameters as the previous run.

8.5.32 $RUN5 COMMAND

Used to initiate a sequence of 5 $BITE runs. Only the first run prompts the user for run time parameters. The following 4 runs utilize the same run time parameters as the first.

8.5.33 $SCR COMMAND

Used for selecting or deselecting the 20 stage feedback scrambler and descrambler.

8.5.34 $SETUP COMMAND

Used to initialize the complete system. The user is prompted for selections on all of the system options.

8.5.35 $TAP COMMAND

Used to set the gains on the various taps in the 12 section channel model for each receiver.

8.5.36 $TDM COMMAND

Used to select or deselect the TDM option. If selected, the user is prompted for the TDM parameters. If selected, TDM run time statistics are supplied at the end of any $BITE, $RUN, or $RUN5 run.

8.5.37 $TDMINT COMMAND

Used to invoke a TDM random startup study. Averages the initial synchronization time for random mux/demux startup. The user is prompted for the noise characteristics and number of runs to be averaged in the study.

8.5.38 $VIEW COMMAND

Used to display all currently selected options.

8.5.39 ESCAPING FROM I/O

If the user desires to return to the INDEXH or INDEX2 program monitor at any time during an input request, a "/*" combination in columns 1 and 2 will accomplish this. Care must be utilized in doing this. If, for instance, a routine requests 5 parameters and the user escapes back to the program monitor after answering the first 2 questions, an inconsistent set of parameters will be stored for that data set. It is suggested after utilizing the escape, to go back and re-invoke the input routine to enter a consistent data set.

8.6 ANALOG USER DISPLAYS

Output of the transmission system simulation is not only made to the Tektronix terminal, but also to the eight-channel stripchart recorder in the form of analog signals vs. time. The simulation variables are all available for output to the stripchart recorder. A typical set of eight simulation variables to the stripchart recorder are:

o 1 Logarithmic fading channel envelope, Receiver A

o 2 Logarithmic fading channel envelope, Receiver B

o 3 Bit errors, Receiver A

o 4 Bit errors, Receiver B

o 5 Bit errors, Diversity

o 6 AGC amplitude, Receiver A

o 7 AGC amplitude, Receiver B

o 8 Status of diversity selector.

Simulation variables such as the outputs of the Offset Threshold Monitor (OTM) for receivers A and/or B, the Baseband Equalizer (BBE) tap coefficient values, or the coincidences between the diversity switch status and the RF envelope power may be substituted for one or more of the above simulation variables.

9. MARTIN MARIETTA CORPORATION

Martin Marietta Corporation is a multi-product corporation that provides materials and systems basic to the needs of the United States. It was formed in 1961 by the amalgamation of the Glenn L. Martin Company, a pioneer aircraft company, and the American Marietta Company, a long established, diversified company. Today, the corporation is comprised of four operating companies: aerospace, aggregates, cement, and chemicals.

9.1 ORLANDO AEROSPACE DIVISION

The Orlando Division of Martin Marietta Aerospace was formed in 1956 to provide for the development, production and test of high quality tactical missiles and communication oriented eletronic systems and components.

9.2 TECHNICAL COMPUTING CENTER BACKGROUND

Orlando Division scientific computational experience is centered in the Technical Computing Center (TCC). The TCC department is composed of two physical sites located at the Sand Lake Road Complex (SLRC) and the new site at the Electronics Systems Center (ESC). The TCC has extensive experience in simulation, analysis, design, and evaluation of electronic and communication systems and techniques. In particular, this computing center has concentrated on sophisticated simulations of these systems throughout the electromagnetic spectrum, including investigations reaching into the microwave and millimetric spectral area.

Extensive computer and library facilities are available to aid in the design and evaluation of performance of proposed studies and contracts. The Orlando Division is also fully equipped with the most advanced research and development, test and manufacturing facilities. These laboratories are supported and complemented by other on-site facilities such as environmental laboratories, engineering prototype facilities, climatic chambers, and heavy structural test facilities.

The TCC is comprised of specialists with advanced degrees and experience in a wide range of scientific disciplines. A partial list of the fields of specialization of these personnel follows:

Communication Systems Analysis
Airplane, Aerospace, Reentry, Land and Marine Vehicles
Target Identification and Tracking
Guidance and Control
Telemetry Data Processing
Information Processing
Nuclear Power Generation
Circuit and Network Analysis
Electromagnetic Phenomena
Ray Tracing
Chemical Processing
Life Sciences and Physiological Systems
Ecological Resources and Relationships
Economics
Operations Research
Biomedical Research
Hydraulic Transient Analysis
Electric Power Transmission
Computer Aided Design
Computer Aided Engineering
Task Oriented Software Development and Analysis
Autopilot Design
Mechanical Systems Analysis
Structures
Computational Science

The TCC personnel have developed application software, performed system management functions, done configuration control, investigated new technologies, developed hardware interfaces, and maintained both the hardware and software portions of the computer systems for their equipment. As a result, the TCC staff has developed the skills required to directly contribute to a broad spectrum of engineering investigation and also manage a broad spectrum of computer technologies. These skills are unique in that they represent a "group" dedicated to applying computer resources to the solution of engineering problems.

9.3 TECHNICAL COMPUTING CENTER FUNCTIONS

The Technical Computing Center is used for missile control and guidance studies, communication system analysis, hydrodynamic analysis, mechanical system studies, power plant analysis, flight test data reduction, and various scientific computing assignments. The TCC is one of the worlds

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largest and most experienced multiple-hybrid computing installations. The center can handle three large-scale hybrid simulations simultaneously since it contains one Interdata 8/32-EAI 8800 hybrid computing system, one Interdata 8/32-EAI 780-8800 hybrid system, and with the recent addition of an EAI Simstar system, simulations may be interchanged in seconds.

In addition to the hybrid systems, TCC's functions and capabilities cover a large segment of computing technologies covering minicomputer, hybrid-computer, data acquisition, and engineering workstation technologies for both ESC and SLRC. These technologies include not only the hardware and software but also the skills associated with managing, maintaining, enhancing, networking, and operating that equipment and software. See Figures 9-2 and 9-2 for TCC's SLRC and ESC equipment configurations. The minicomputer systems which are available to the general user community are :

1. One VAX 11/782 dual processor minicomputer at ESC
2. One VAX 8600 minicomputer at ESC
3. One Perkin-Elmer 832 minicomputer at ESC
4. Two VAX 11/780 minicomputers at SLRC
5. Two VAX 11/785 minicomputers at SLRC
6. One VAX 8600 minicomputer at SLRC
7. One SEL 32/9780 minicomputer at SLRC
8. One Perkin-Elmer 3240 minicomputer at SLRC
9. Two Perkin-Elmer 832 minicomputers at SLRC

9.4 TCC ESC OPERATIONS

(See Figure 9-1)

The VAX 11/782 minicomputer, system 10, and the new VAX 8600, system 11, are clustered together and are equipped with the following equipment and peripherals:

VAX 11/782 -

1. Eight megabytes of 16k Metal Oxide Semiconductor (MOS) memory
2. One megabytes of 16k local memory
3. One TE-16 800/1600 bpi dual density mag tape drive
4. One RP07 516 megabytes disk drive
5. One RM05 256 megabytes disk drive
6. One DAC 1210 1600 lpm lineprinter
7. Sixteen direct ports
8. Thirty-two indirect ports
9. ETHERNET communication link
10. DECnet communication link
11. VAXcluster computer interconnect

VAX 8600 -

The VAX 8600 minicomputer, system 11, can be described as:
1. Twelve megabytes of ECC MOS memory
2. Multipurpose communication controllers (8 direct ports)
3. Ninety-six DMA asynchronous multiplexer (RS232 direct ports)
4. ETHERNET communication link
5. VAXcluster computer interconnect
6. One operator console and hardcopy terminal

CLUSTER -

1. Six RA81 456 megabytes disk drives (2.7 gigabytes)
2. One TA78 1600/6250 dual density tape drive
3. One TU78 1600/6250 dual density tape drive
4. One 1600 lpm lineprinter

HYBRID -

The hybrid computer system in TCC at ESC is system 90. It is described by:

1. System 90 Perkin-Elmer digital computer
2. Three EAI 8800 analog computers
3. One MFTP
4. One EAI 8930 interface

The Perkin-Elmer 832 minicomputer, system 90, is equipped as follows:

1. One megabytes core memory
2. One control console
3. One card reader
4. Two mag tape drives
5. Two 80 megabytes disk drives
6. One 800 lpm lineprinter
7. One local port
8. Two indirect ports

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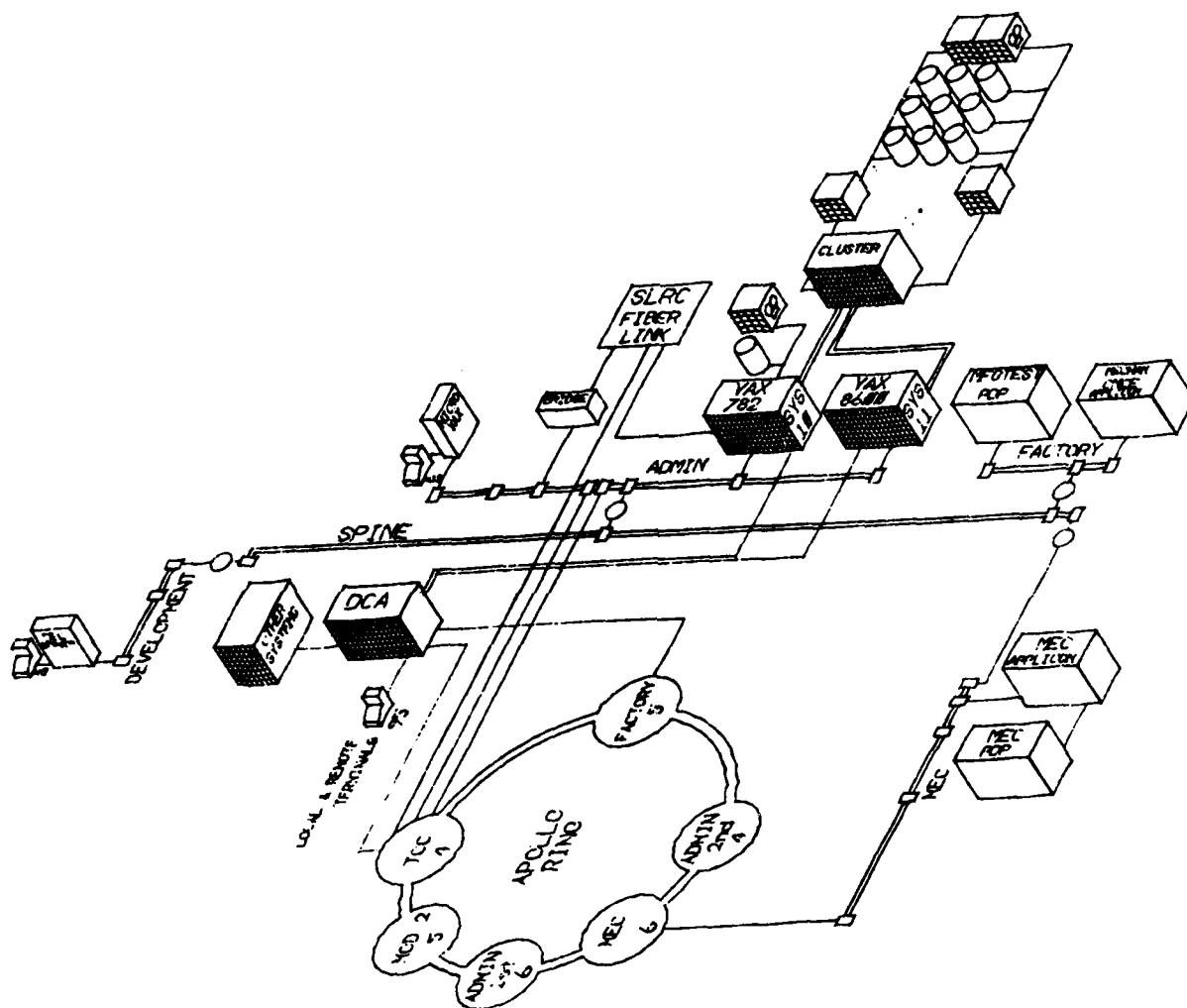
Figure 9-1 MMOA ELECTRONICS SYSTEMS CENTER

9.5 TCC SLRC OPERATIONS

(See Figure 9-2)

VAX 11/780 -

The VAX 11/780 minicomputer, system 21, is housed in a TEMPEST approved room in TCC and can be operated in a dedicated classified mode with a clearance up to SECRET. A TOP SECRET clearance has been applied for and is pending. When the computer is not scheduled for classified operation it is DECneted with the SLRC cluster. System 21 has the following special features:

1. TEMPEST approved
2. SECRET approved, TOP SECRET pending
3. APPLICON editor 3-D interactive graphics system
4. APPLICON solids modeling II package
5. APPLICON surface modeling package
6. APPLICON database manager
7. IGES pre and postprocessor utilities
8. Bill of materials

The VAX 11/780, system 21, hardware description is:

1. Eight megabytes of 64k MOS memory
2. Two RP06 167 megabytes disk drives
3. Three RA60 205 megabytes disk drives
4. One TE16 800/1600 bpi dual density mag tape drive
5. One 1200 lpm lineprinter
6. Eight direct ports
7. Thirty-two indirect ports
8. Two APPLICON raster scan work stations
9. Two RAMTEC 9400 graphical stations
10. One CALCOMP 965 line plotter
11. DECnet communication link
12. One CI780 cluster interconnect port

VAX 11/785 -

The remaining VAX systems are clustered together and are linked to other systems throughout SLRC via ETHERNET. The VAX 11/785 minicomputer, system 40, consists of:

1. Eight megabytes of 64k MOS memory
2. One LP27 1200 lpm band lineprinter
3. One CI780 cluster interconnect port
4. Eight direct ports
5. Thirty-two indirect ports

VAX 11/780 -

The VAX 11/780 minicomputer, system 41, consists of:

1. Eight megabytes of 64k MOS memory
2. One LP27 1200 lpm band lineprinter
3. One CI780 cluster interconnect port
4. Eight direct ports
5. Thirty-two indirect ports

VAX11/785 -

The VAX 11/785 minicomputer, system 42, consists of:

1. Eight megabytes of 64k MOS memory
2. One LP27 1200 lpm band lineprinter
3. One CI780 cluster interconnect port
4. Eight direct ports
5. Thirty-two indirect ports

VAX 8600 -

The VAX 8600 minicomputer, system 43, consists of:

1. Twelve megabytes of ECC MOS memory
2. Multipurpose communication controllers (8 direct ports)
3. Ninety-six DMA asynchronous multiplexer (RS232 direct ports)
4. ETHERNET communication link
5. VAXcluster computer interconnect
6. One operator console and hardcopy terminal

CLUSTER -

1. Twelve RA81 456 megabytes disk drives (5.47 gigabytes)
2. One TA78 1600/6250 dual density tape drive
3. One TU78 1600/6250 dual density tape drive

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The VAX computers have the following language compilers, interpreters, and assemblers:

1. ADA
2. BASIC
3. BLISS
4. 'C'
5. ACSL
6. COBOL
7. FORTRAN
8. MACRO
9. PASCAL
10. PL/1
11. DATATRIEVE
12. ADABASE

PERKIN-ELMER COMPUTERS -

The Perkin-Elmer 3240 minicomputer, system 60, is equipped as follows:

1. A 2.5 megabyte of MOS memory
2. One card reader
3. One 1000 lpm lineprinter
4. Four 800/1600 bpi dual density mag tape units
5. Four 80 megabytes disk drives
6. One V80 Versatec plotter
7. Two stripchart recorders
8. Eighteen indirect ports
9. One 675 megabytes disk drive

The Perkin-Elmer minicomputers, systems 70 and 80 respectively are the two digital minicomputers which are the digital elements of two of our four hybrid systems. System 70 is equipped as follows:

1. A 756 kilo byte core memory
2. A control console
3. A card reader
4. Two mag tape drives
5. Two 80 megabytes disk drives
6. A 600 lpm lineprinter
7. A local port
8. Two indirect ports

Systems 80 and 90 are equipped identically as follows:

1. One megabyte core memory
2. A control console
3. A card reader
4. Three mag tape drives
5. Two 80 megabytes disk drives
6. An 800 lpm lineprinter
7. A local port
8. Two indirect ports

Figure 9-2 MMOA SAND LAKE ROAD COMPLEX

9.6 TCC SLRC HYBRID OPERATIONS

(See Figure 9-3)

There are four hybrid computing systems in TCC SLRC as shown in Figure 9-3. System 50 is made of a SEL (System Engineering Laboratories) 3297 minicomputer and three EAI (Electronic Associates Inc) SIMSTAR hybrid computers. The SEL 3297 minicomputer consists of:

1. One 32/9780 computer system with dual processors (CPU and IPU)
2. Four megabytes MOS memory
3. Eight direct ports
4. One 600 lpm lineprinter
5. Two 80 megabytes mini-cartridge disk drives
6. Two 800/1600 dual density tape drives
7. One 300 megabytes disk drive

Some of the features of the SIMSTAR hybrid system are:

1. Ten times faster than previous analogs
2. Ten db more signal/noise resolution
3. More reliable (self testing, adjusting, and maintainence features)
4. Low signal multiplication rescale
5. No patch board
6. Problem change over in milliseconds
7. User friendly (CRT programmed via host using FORTRAN or ACSL)

System 70 hybrid system is:

1. System 70 Perkin-Elmer digital computer
2. Three EAI 781 analog computers
3. One EAI 8800 analog computer
4. One MFTP (MultiFunction Table Processor)
5. One EAI 7930 interface

System 80 is described similarly:

1. System 80 Perkin-Elmer digital computer
2. Three EAI 8800 analog computers
3. One MFTP
4. One EAI 8930 interface

A fourth hybrid system (array processor/digital) consists of the VAX 11/782 system 40 linked to an Applied Dynamics AD10 multiprocessor pipelined computer. The AD10 contains the following :

1. 388 kilobytes of MOS memory
2. MAP memory address processor
3. DEP decision processor
4. ARP arithmetic processor
5. COP control processor
6. NIP numerical integration processor

The AD10 is programmed on the VAX using the hiearchial language MPS10 and then that program is compiled and downloaded to the AD10 by the HIC-RIC interface.
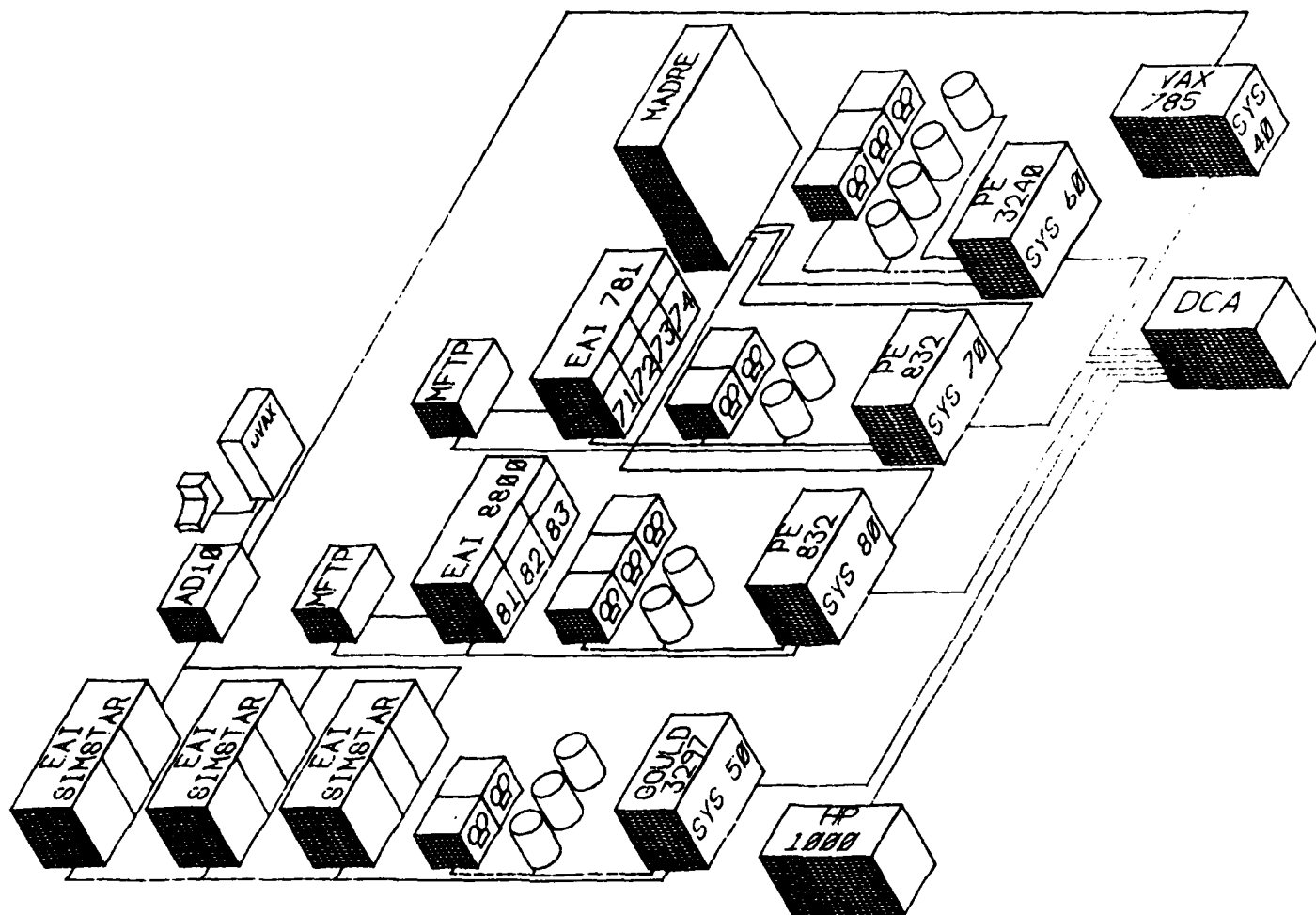
Figure 9-3 MMOA SLRC HYBRID SYSTEMS

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COMMUNICATIONS -

The TCC VAXes are connected to a Local Area Network (LAN) baseband system called ETHERNET. There are two ETHERNET LANs, one at ESC and the other at SLRC, which are connected by DECnet via a T1 fiber optic link. The systems connected to the ETHERNET LANs are SYS10, SYS11, MECVAX, CNCEVX, CAEVAX, LASAR1, LASAR2, LASAR3, MICVAX, SYS21, SYS40, SYS41, SYS42, SYS43 and a SNA gateway to the Martin Marietta Data Systems (MMDS) IBM mainframes. SCICARDS and the Apollo Domain will be added to the ETHERNET LAN this year.

The various minicomputers in TCC are primarily interfaced to the user community through the indirect ports associated with each minicomputer. These ports are connected to three Digital Communication Associates (DCA) 355 network processors. The DCA 355 is a microprocessor based data switch that is used in medium to large full-function networks. Each DCA 355 can support up to 80 trunk lines and provides network management and control with features such as port contention, host selection, multiplexing and routing. The equipment configuration figures provide a representation of the existing TCC communication network. TCC has 304 terminals distributed throughout the user community.

9.7 TCC OBJECTIVES

The requirements for TCC support have grown from the traditional support of systems engineering (simulation and modeling) to include a wide diversity of engineering disciplines, and also, manufacturing, industrial, and engineering administration technological support. This support has included:

1. Acquisition of computer equipment and software

2. Training on VAX, Apollo, Mentor systems , et al

3. Training on TEGAS, SPICE, other application software

4. Evaluation of computers, software, et al

5. Provide systems management, operations, maintenance, software development and support, and configuration management

6. Computer communication hardware acquisition, system management, and network integrity and control

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7. Consultation

The objective of TCC is to be an available expert computer technical resource to all technical areas of Orlando Aerospace and to continue providing simulation expertise to the engineering community.

10. SUMMARY

This report documented work done in compliance with the DCA-100-81-G-0001 contract. Main accomplishments included expanding the fading channel model to include the Nakagami-Rice fading characteristic, incorporating advanced modulation schemes (QAM, PSK and QPR) into the DRAMA simulation and continuing the availability of the DRAMA simulation. Also, new error correction modems were installed to enhance remote capability. The concentration of work is presently focused toward enhancing the design and development of Modteq on the Simstar and maintaining the existing simulations. Robert Orr of DCEC used the DRAMA simulation successfully in determining baseband performance.

11. APPENDIX A: AN/FRC-170(V) SCHEMATICS

CONSOLE 73 PAGE 1 of 6
BOARD 724

CONSOLE 73 PAGE
BOARD 724 3-6
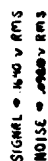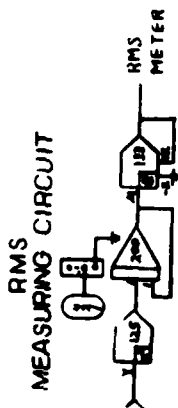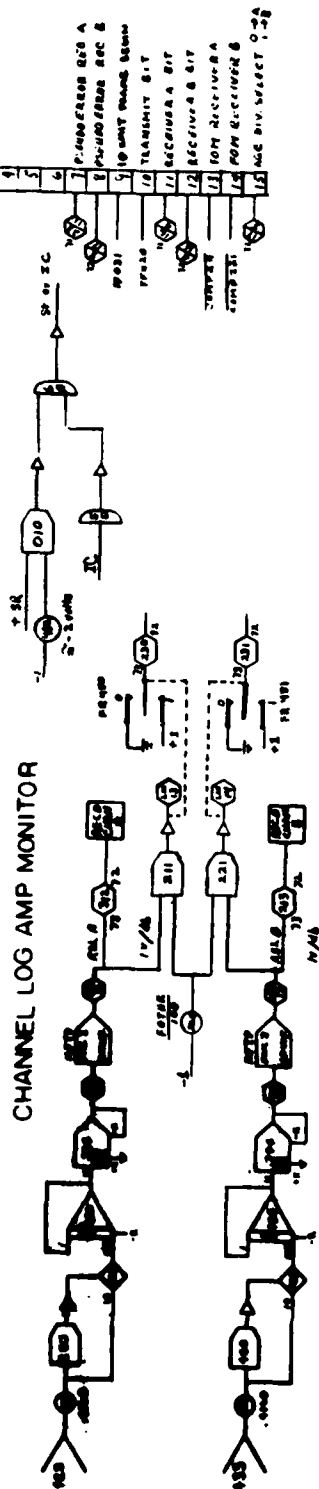
RF FILTER #1

RF FILTER #2

TWT

A-4

CHANNEL MEDIA MODEL

CONSOLE 73 PAGE 4~6
BOARD 724

CHANNEL A

CHANNEL B

TEST AND DISPLAY CIRCUITS

HYBRID COMPUTATIONS DEPARTMENT

PSD f FREQUENCY RESPONSE

IF FILTER 15

CONSOLE 711 PAGE
BOARD 1 OF 7

ABSOLUTE VALUE
CIRCUIT

PEAK RIDER

AGC CIRCUITRY

VARIABLE GAIN CIRCUIT

AGC
CONTROL VOLTAGE

CONSOLE 71 BOARD 711
PAGE 2 OF 7

DEMODULATOR LOOP

FILTER 13 'I' BASEBAND

PPL FILTER

FRED CORRECTION

RECEIVE OSCILLATOR

AMPLITUDE CORRECTION

FILTER 14 'Q' BASEBAND

ADAPTIVE THRESHOLDS AND DATA ESTIMATORS

CONSOLE 71 BOARD 711
PAGE 3 OF 7

A-10

CONSOLE 711
BOARD PAGE 4..7
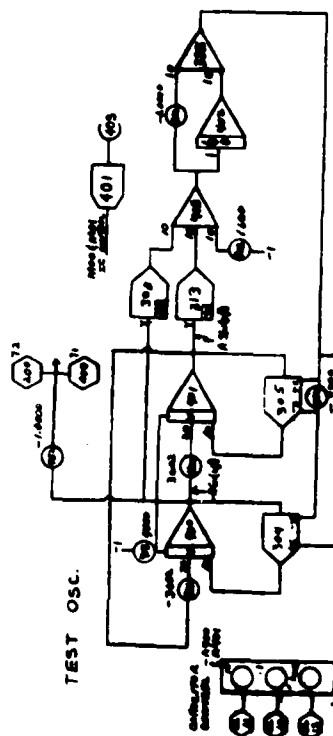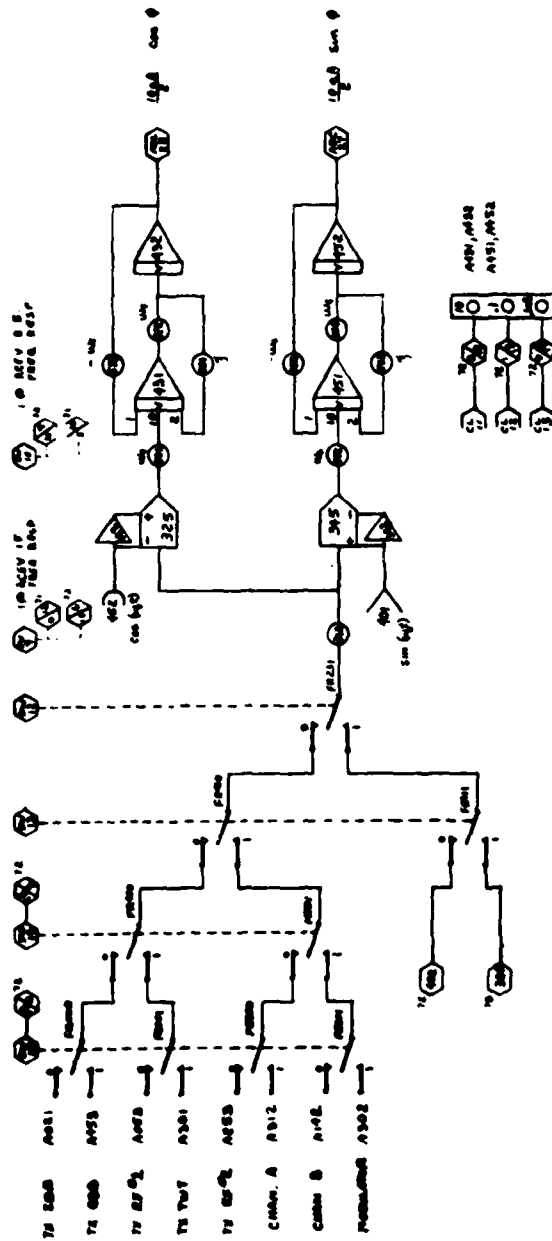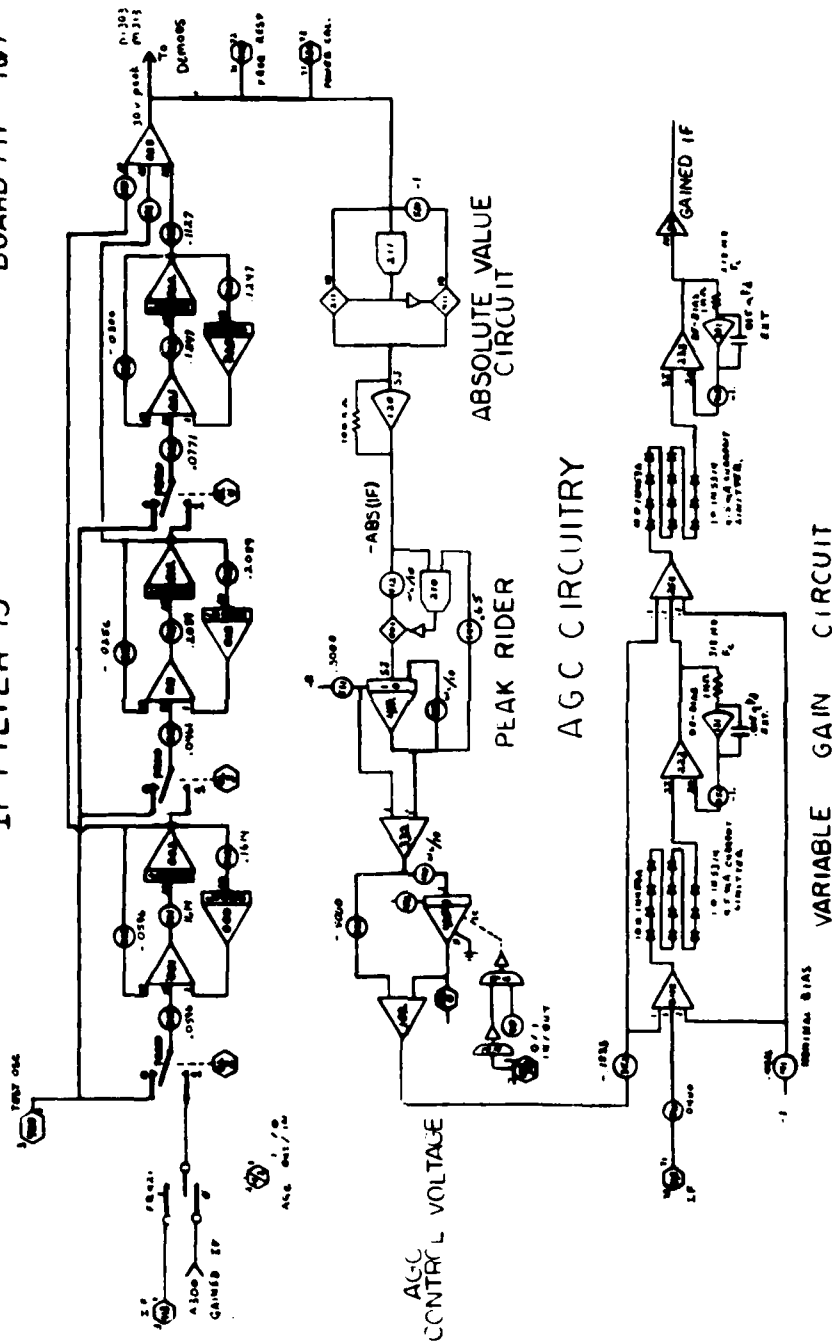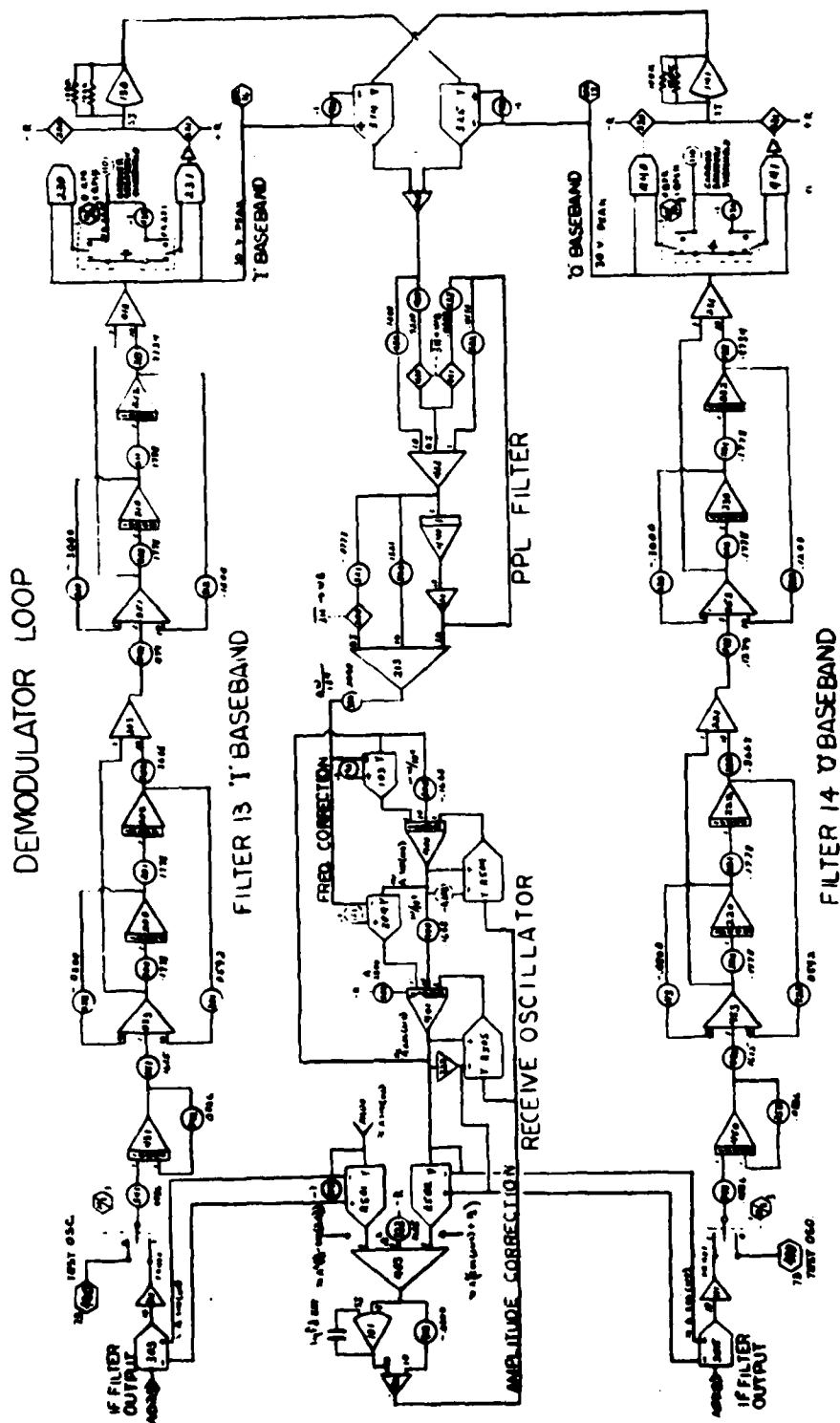
CLOCK RECOVERY PLL

LOCK DETECTION
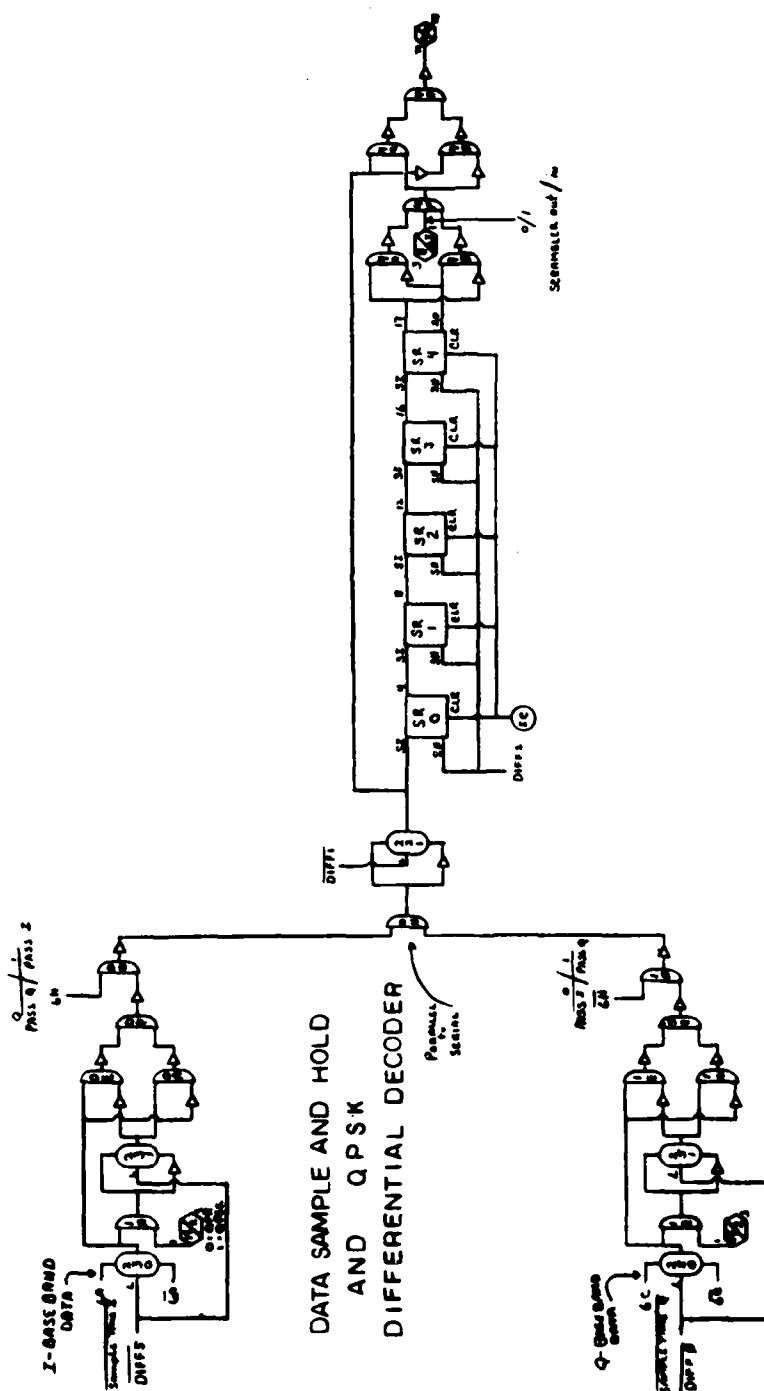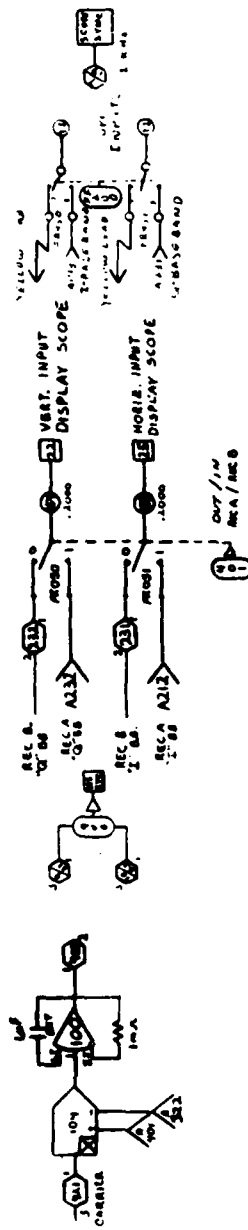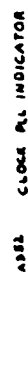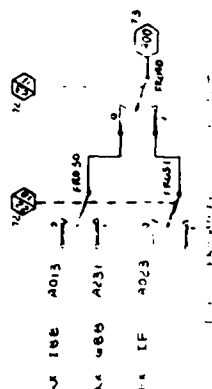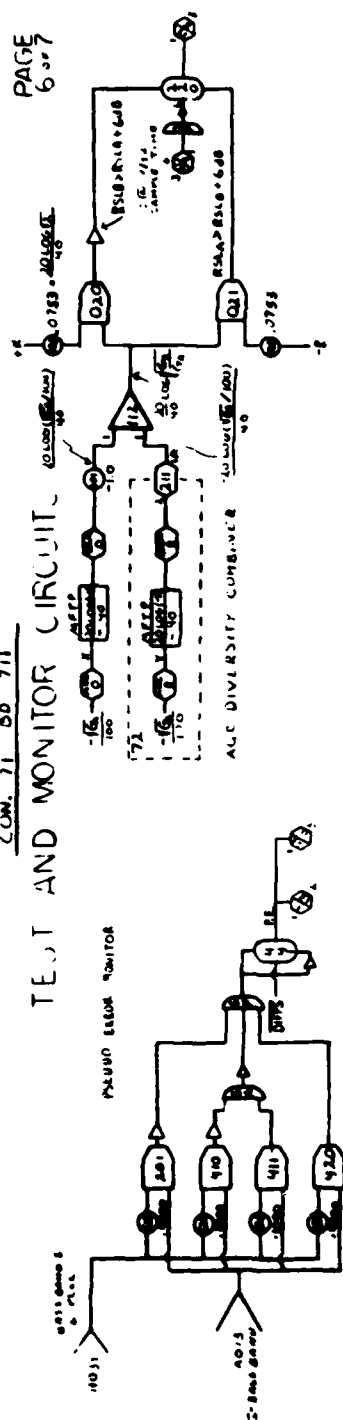
A-11

DATA REGENERATION

DATA SAMPLE AND HOLD
AND QPSK
DIFFERENTIAL DECODER

TEST AND MONITOR CIRCUIT

A-13

CHANNEL MEDIA MODEL

Σ CHANNEL NOISE

IF FILTER 11

CONSOLE 72
BOARD 721   PAGE 1 of 7

ABSOLUTE VALUE CIRCUIT

PEAK RIDER

AGC CIRCUITRY

AGC CONTROL VOLTAGE

VARIABLE GAIN CIRCUIT

DEMODULATOR LOOP

FILTER 9 'I' BASEBAND

'I' BASEBAND

PLL FILTER

FREQ CORRECTION

RECEIVE OSCILLATOR

AMPLITUDE CORRECTION

IF FILTER
OUTPUT

IF FILTER
OUTPUT

FILTER 10 'Q' BASEBAND

'Q' BASEBAND

ADAPTIVE THRESHOLDS AND DATA ESTIMATORS

"Q" DATA ESTIMATOR

"I" DATA ESTIMATOR

BB ZERO CROSSING THRESHOLD

LOCK DETECTOR

DATA REGENERATION

DATA SAMPLE AND HOLD
AND
DIFFERENTIAL DECODER QPSK
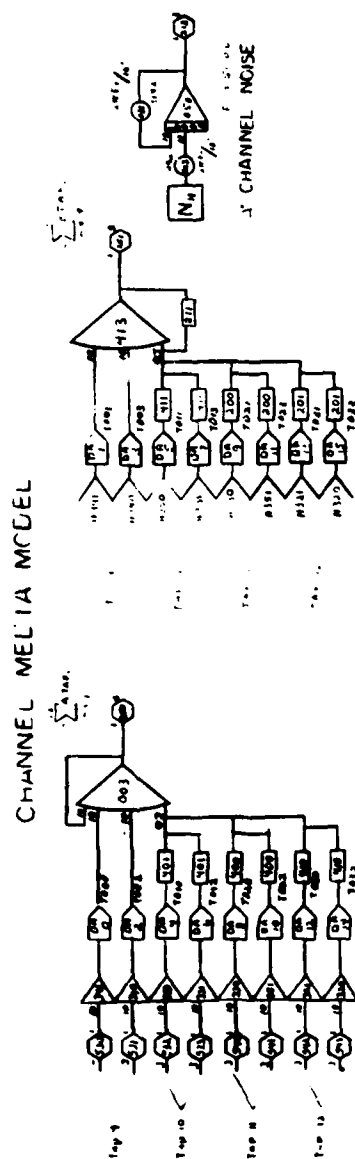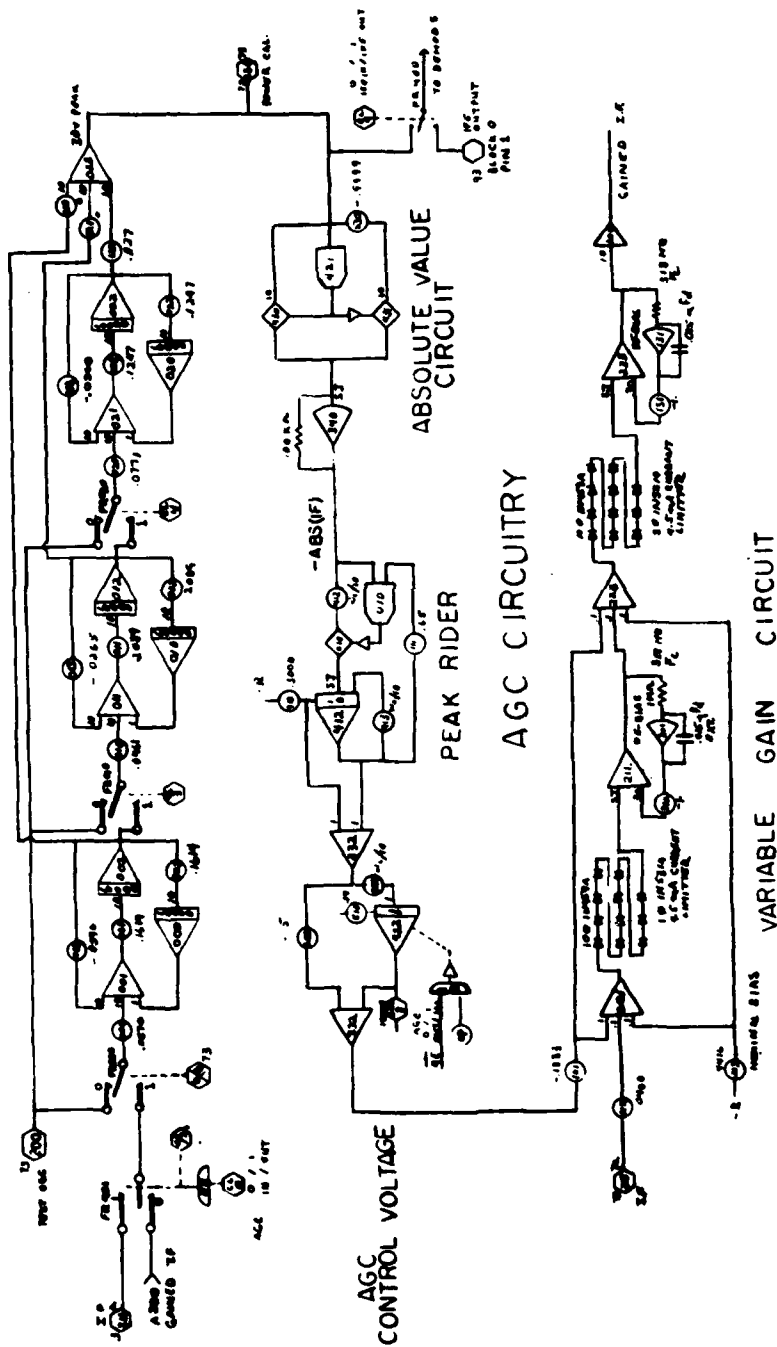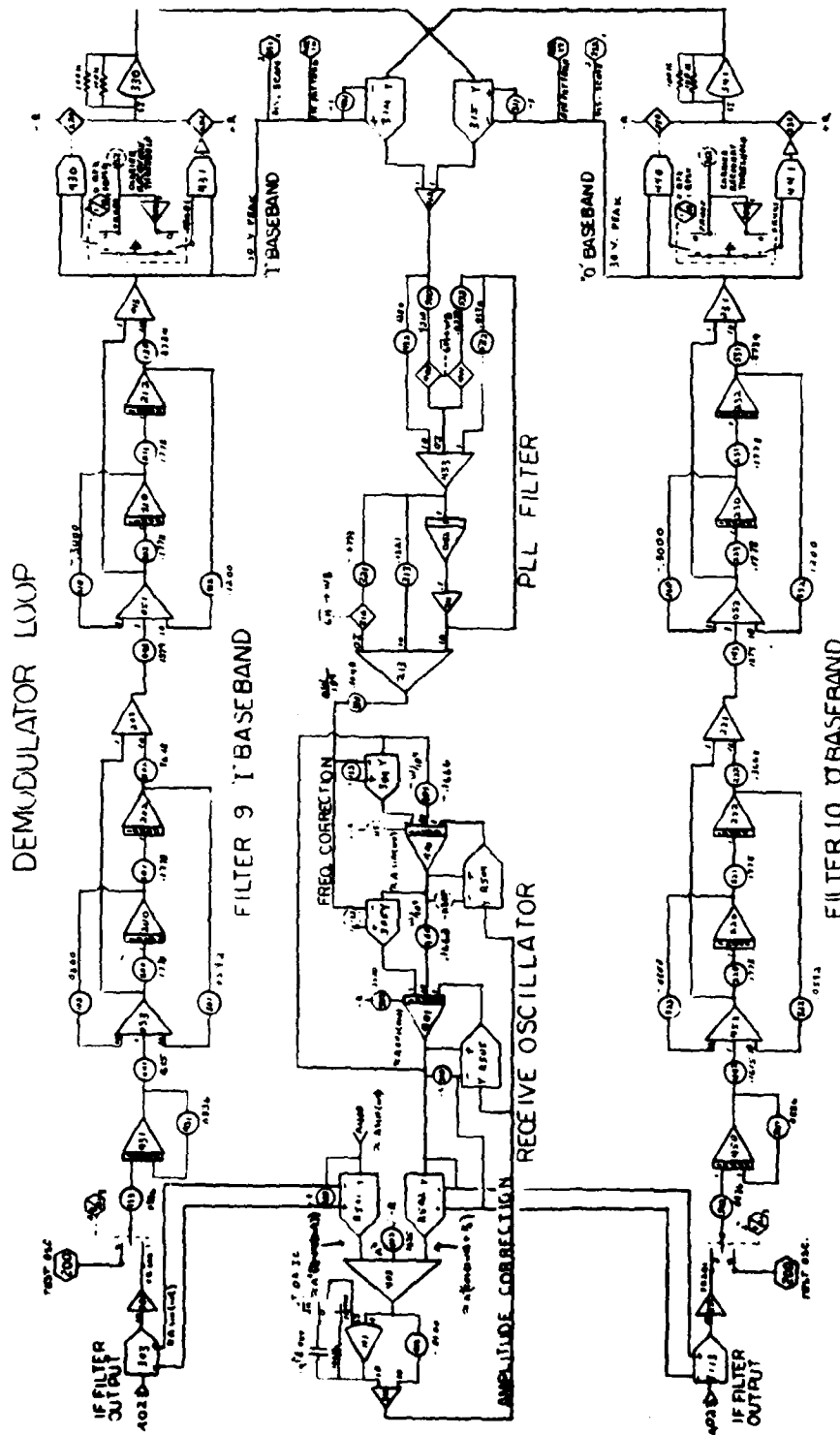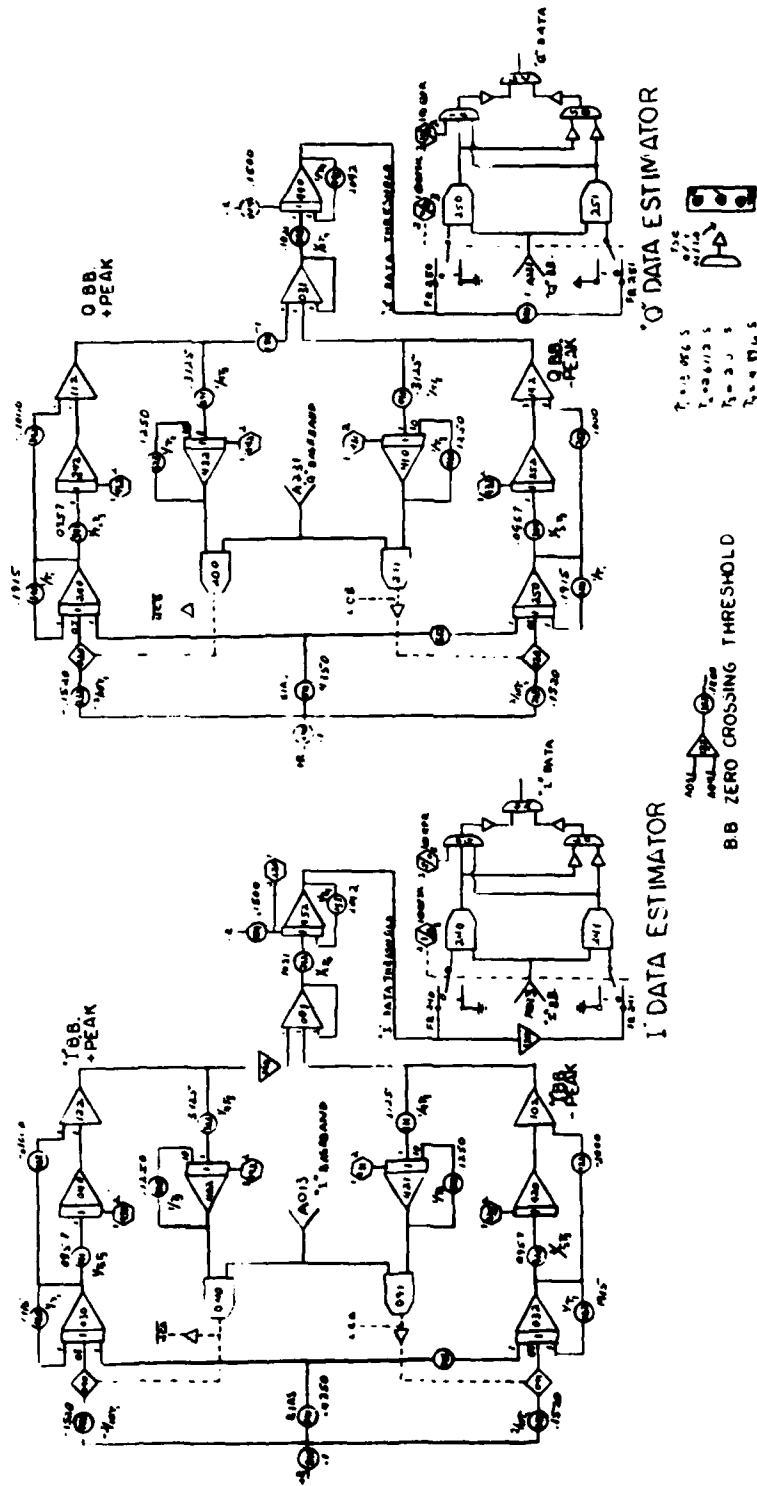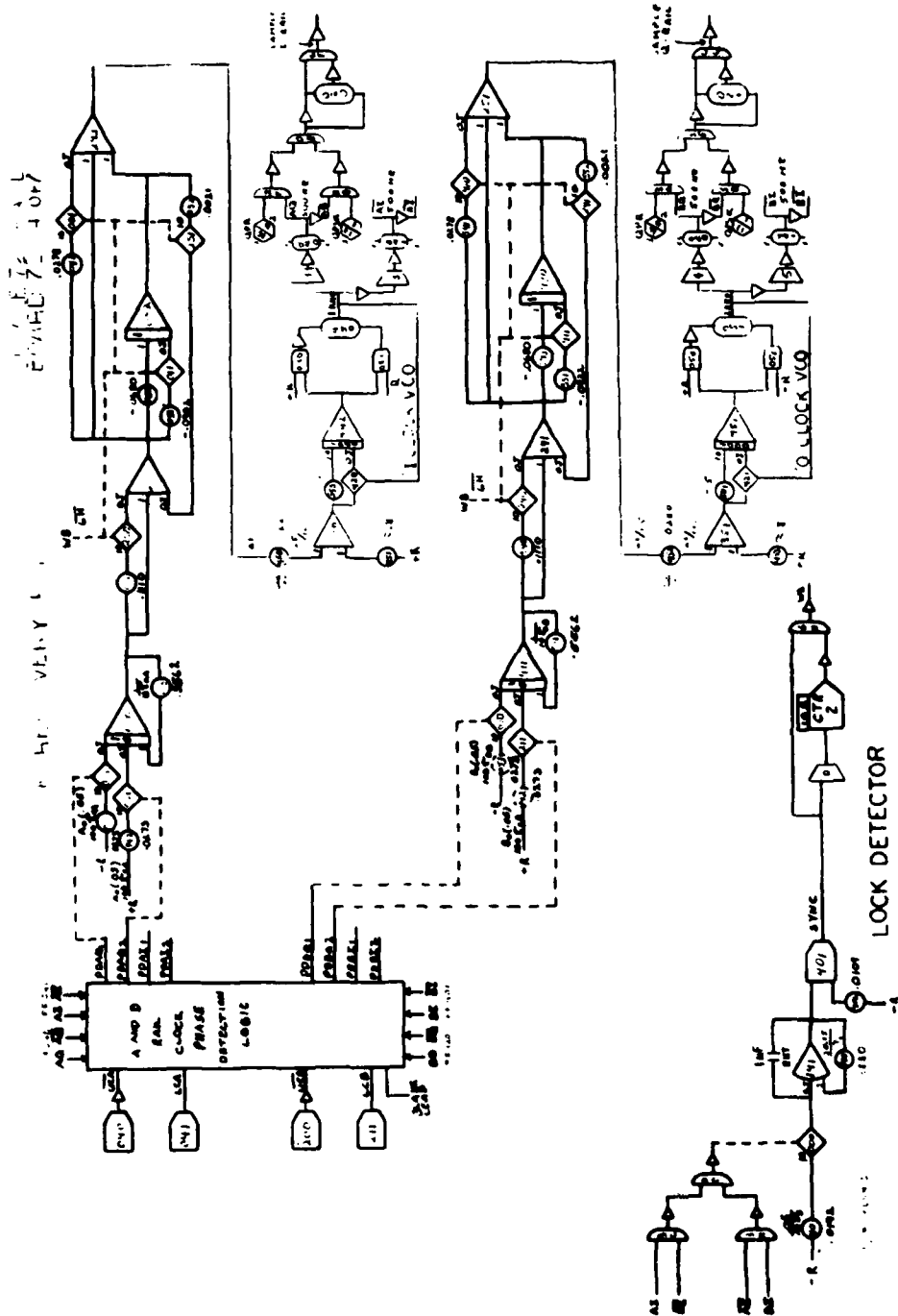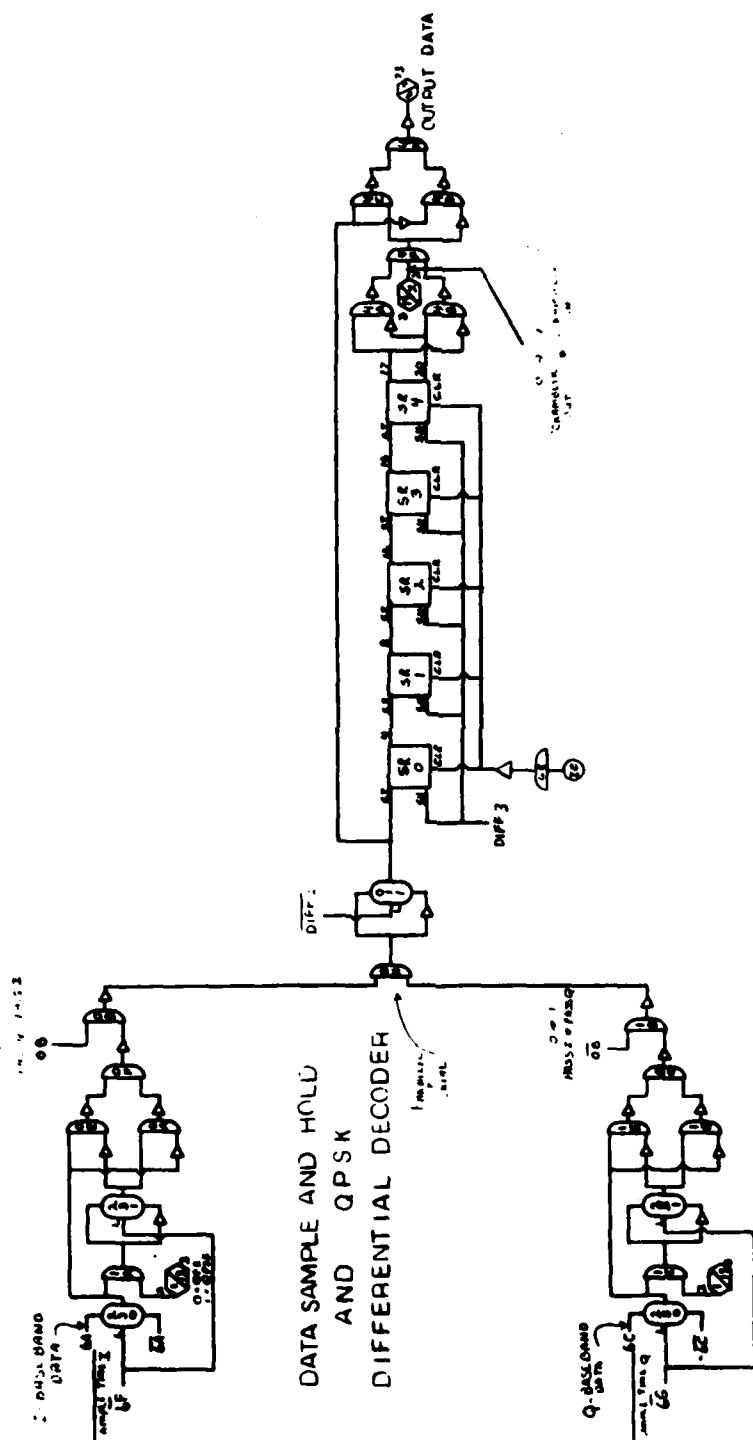
TEST AND MONITOR CIRCUITS

CHANNEL MEDIA MODEL

CHANNEL NOISE

HYBRID COMPUTATIONS DEPARTMENT
ORLANDO DIVISION

IF EQUALIZER

SLOPE EQUALIZER SECTIONS

A.L.C.

SLOPE EQUALIZER GAIN COMPENSATION
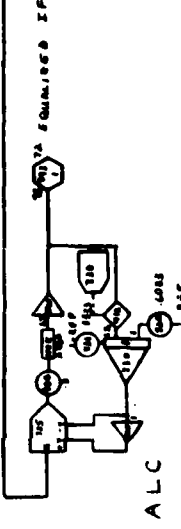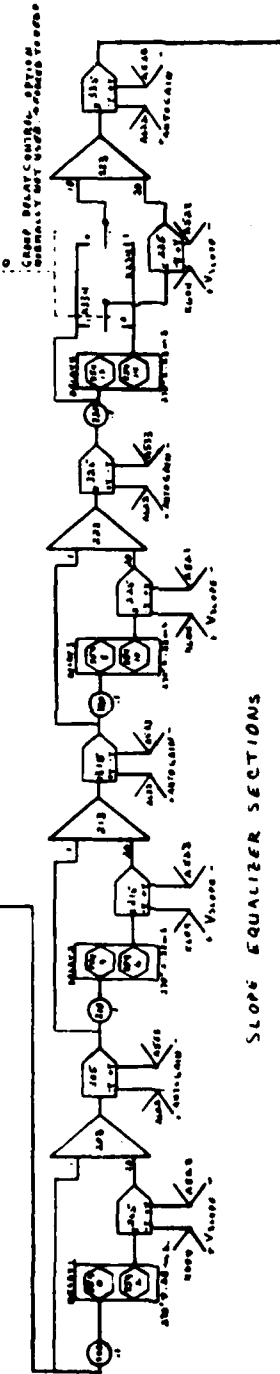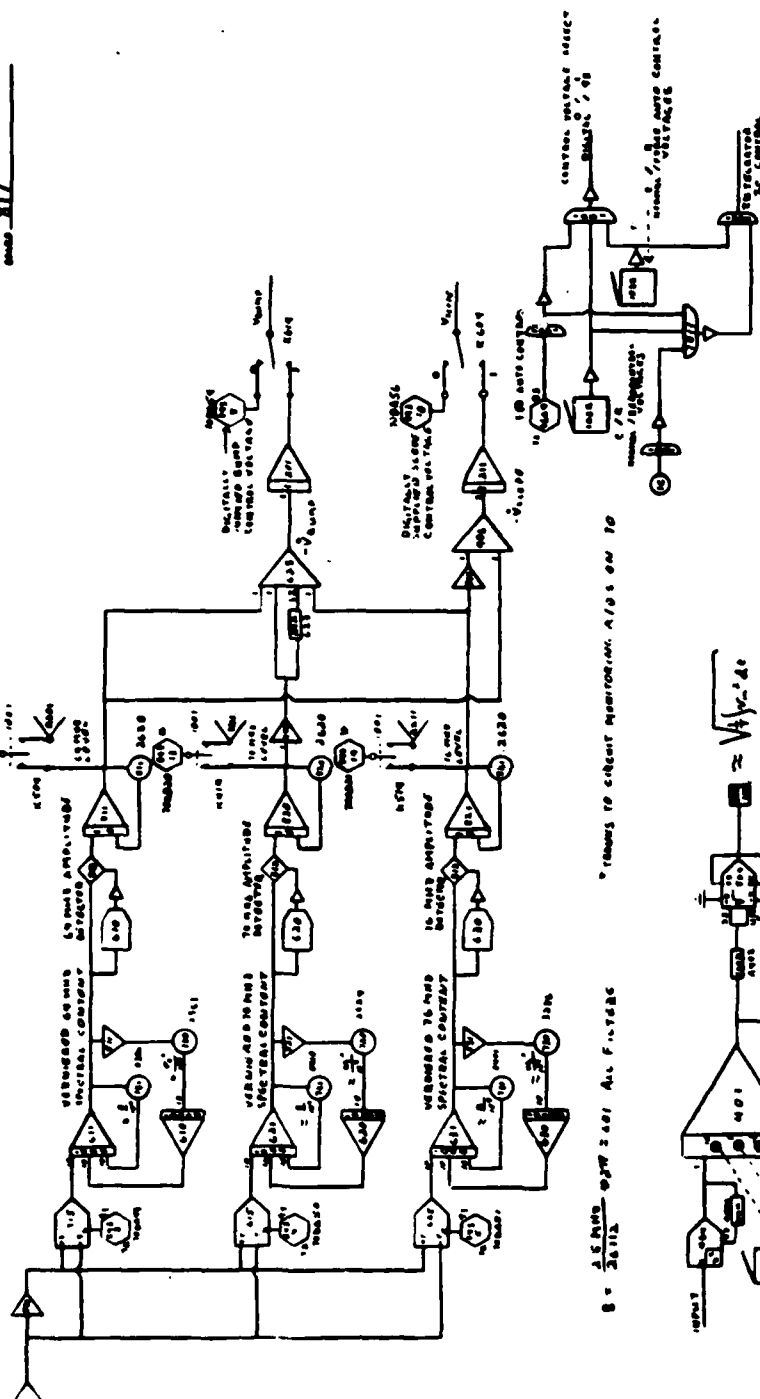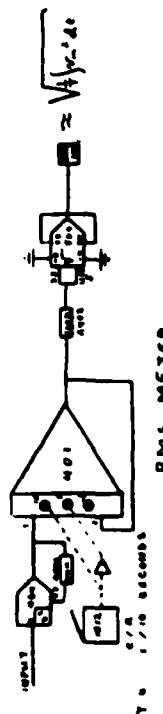
12. APPENDIX B: BASEBAND EQUALIZER SCHEMATICS

1 MILLISECOND DELAY

DELAY 1

1 MILLISECOND DELAY

DELAY 2

DELAY LINES

B-2

CLOCK RECOVERY

B-3

CARRIER RECOVERY

B-4

CONTROL AND MONITOR

0 TO 1
TRANSITION
DETECTOR

HYBRID
SYNC
PULSE

RESET 88E

S 451 R

3G

CL
3

NB TRIGGER

1H

MUX

1D   1C

PBFF0
0 / 1
0, 90 / 70

DW0 70 NB TRIGGER

80, 90 NB TRIGGER

24

RECEIVED DATA

3H

MUX

3C   3D

PBFF0
0 / 1
0, 90 / 70

DW1 70 RECEIVED DATA

80, 90 RECEIVED DATA

25

SKIP DFE

S 450 R

5C

CL
2

SKIP FFE

S 441 R

5D

CL
1

LW DW

0/2   71

5F

73

S 031 R

DATA(t-DELAY)

16/4   73

71

S 040 R   1

DELAY
SELECT
TOGGLE

5A   5E

5B

MUX

DATA(t)

S 030 R   DATA(t-.5msec)

DATA(t)

S 041 R

TIMER 0.C

5

CLOCK(t-.5msec)

DATA 3H

TIMER 0.A
CLOCK(t)

1

SENSES OUTPUT DATA TRANSITIONS OCCURRING
AT OR NEAR HYBRID SYNC TIME. IF ONE OCCURS,
DATA IS RETIMED BY 0.5 MILLISECONDS.

FRAME PULSE TIMER 0.A   0   0
SKIP FFE FF441   1   1
SKIP DFE FF450   2   2
RESET FF451   3   3
HALT PBFF3   4   4
NARROW BAND FF440   5   5
SEPARATE ERRORS GPR 5.3 6   6
SEPC01 GPR 5.2   7   7
                         8   8
                         9   9
                        10   10
                        11   11
                        12   12
                        13   13
                        14   14
                        15   15

1D NB TRIGGER
SC RECEIVED DATA

STRIPCHART 1

K010 CQ0   A
K011 CQ1   B
K210 DI0   C
K211 DI1   D
            E
            F
            G
            H

STRIPCHART 0

K000 CI0   A
K001 CI1   B
K200 D00   C
K201 D01   D
K020 W1   E
K021 W2   F
K220 W3   G
K221 W4   H

B-5

WIDEBAND NARROW BAND SELECTION

TRUNKING DIAGRAM

FEED FORWARD EQUALIZER

B-8

13. APPENDIX C: SIMSTAR SOFTWARE

This appendix contains the listings of the Simstar software which has replaced the normal schematic diagrams which have been included in the past year end reports. Since the Simstar is software driven as opposed to patch driven, there is no necessity for schematics. The same information and more can be obtained by studying the listings provided.

The following listing contains the source used to implement the analog portion of the hybrid program:

```
*PSP 1, 0, ERR = ALL
*TITLE
QAM/QPR
*INPUT (6)

PROGRAM

    'CFREQ IS FREQ. OF CARRIER OSC.(HZ),TMAX IS SIMULATION END TIME(SEC)'
    'RS IS SYMBOL RATE, GAIN1-GAIN4,SSGAIN,K1 ARE'
    'PHASE LOCK LOOP FILTER GAINS'

    'OBETA(TIMSCL)'


        CONSTANT   RS = 26.112E6, PI = 3.14159, XTRABW = 1.25
        CONSTANT   SMTHEX = .2, ONE = 1.0, ZERO = 0, MINUS = -1.0
        CONSTANT   TIMSCL = 26112, A = 1, CFREQ = 70.E6, OSET=.5
        CONSTANT   OSET = .5, TINT = .0000100001, TSAMP = .0001
        CONSTANT   FRSWC=1,PIE=3.14159,SAMFCO=159155


        'OPARAMETER        TIMSCL, XTRABW, OSET, VARG'

        'OMAXVAL   TIMSCL = 26112.E2, XTRABW = 2, OSET=.5, VARG=5'
        'OMINVAL   TIMSCL = 26112   , XTRABW = 1, OSET=0 , VARG=0'

    INITIAL
        TS = 1/RS
        SMTHFC = ( 1 + SMTHEX )*RS/2
        SMTHWC = 2 * PI * SMTHFC
        OMEGA1= 2 * PI * CFREQ
                          LPFWC        =    PI   *   RS   *   XTRABW
```

```
        AMPSQ = A**2

        GAIN = D/TINT - VARG
        QIC = OSET*D
        THRESH = 0.5*D
        SAMPL = TSAMP*TIMSCL/26112
        FRSWC = 2*PIE*SAMFCO
     END

     DYNAMIC

        TGRAY = W
        TGRDIF = X
        Y = TCLOCK
        OMEGA = DUM
        FTYPE = DUM2
        FLT1IN = DUM3

        DERIVATIVE
            '@PARALLEL'

            'CARRIER OSCILLATOR'

        '@SCALE    SINE = 1, COSINE = 1, F = .25'

            SINE = INTEG(OMEGA1 * COSINE + IN2,0)
            COSINE = INTEG(-OMEGA1 * SINE + IN3,A)
            IN2 = SINE * G * OMEGA1
            IN3 = COSINE * G * OMEGA1
            G = F + E
            F = INTEG(E,0)
            E = AMPSQ - SINE**2. - COSINE**2.

     'TRANSMITTER LOGIC & CLOCKING'

     LOGICAL    PRST5, TCLOCK, TRSD2, LAD10S

     INTEGER CLKCNT

     'PULSE AT 5 TIMES SYMBOL RATE'

        PRST5 = CLOCK( TS/5*TIMSCL )

     'LOGIC  AD10 100 MICROSEC. SYNC PULSE AT 5 TIMES SYMBOL RATE'

        LAD10S = MONO( 100E-6 , PRST5 )
```

```
'ANALOG AD10 100 MICROSEC. SYNC PULSE AT 5 TIMES SYMBOL RATE'

   AAD10S = RSW( LAD10S , 1 , -1 )

'PULSE AT SYMBOL RATE: TRANSMITTER CLOCK'

   TCLOCK,CLKCNT = DNCTR( 4 , PRST5 , MODE(IC) )

'LOGIC & ANALOG SQUARE WAVE AT HALF THE SYMBOL RATE'

   TRSD2  = SRTEFF(.FALSE.,.TRUE.,.TRUE.,TCLOCK)
   SRSD2  = RSW( TRSD2 , 1 , -1 )

'SMOOTH THE AD10 BASEBAND FILTER OUTPUTS WITH 600. HZ CUTOFF'
'AD10I & AD10Q ARE I & Q BASEBAND AFTER PARTIAL RESPONSE'
'FILTERING ON THE AD10'

'@SCALE   TIBBD = 1, TQBBD=1,TIBB=1,TQBB=1,AD10I=1,AD10Q=1'

CONSTANT TBBGAN=1,SMTHZT=.65

'@MAXVAL TBBGAN=1,SMTHEX=.2'

   TIBBD=INTEG(AD10I*SMTHWC*TBBGAN - IFDBK1 - IFDBK2,0)
   IFDBK1 = 2*SMTHZT*SMTHWC*TIBBD
   IFDBK2 = SMTHWC*TIBB

   TIBB =INTEG(SMTHWC*TIBBD,0)

   TQBBD=INTEG(AD10Q*SMTHWC*TBBGAN - QFDBK1 - QFDBK2,0)
   QFDBK1 = 2*SMTHZT*SMTHWC*TQBBD
   QFDBK2 = SMTHWC*TQBB

   TQBB =INTEG(SMTHWC*TQBBD,0)

 'TIBB & TQBB ARE AD10I & AD10Q AFTER SMOOTHING'

     '@SCALE TGRDIF=1.0, TGRAY=1,TGREY=1'

   LEVBUF=TGRDIF+ZERO*TGRAY
     TGREY = TGRAY + ZERO

     'MODULATION OF BASEBAND'

         MODI = TIBB * SINE
         MODQ = TQBB * COSINE
```

```
'ADD RAILS TO PRODUCE TRANSMITTER OUTPUT'

'@SCALE QUAD=1.0'

'@PARAMETER TGAIN'
'@MAXVAL TGAIN=2'
'@MINVAL TGAIN=0'
CONSTANT TGAIN=0.5

    QUAD = .707*(MODI + MODQ)
    TIF = QUAD * TGAIN

'CHANNEL MODEL SECTION'

'@SCALE NOISE=1'
'@PARAMETER EBN0,SCOEF,NCOEF'
'@MAXVAL EBN0=100    , SCOEF=1.0, NCOEF=10 '
'@MINVAL EBN0=0, SCOEF=.01, NCOEF=.001'
CONSTANT SCOEF=1, NCOEF=0

' *** OSCILLATOR *** '

'@MINVAL OMEGA=1'
'@MAXVAL OMEGA=15.E8'
'@SCALE COS1=1.0 , SIN1=1.0,INTERR=1,ERR=1'

    SIN1 = INTEG(OMEGA*COS1-FC*SIN1*OMEGA,0.0)
    COS1 = INTEG(-OMEGA*SIN1-FC*COS1*OMEGA,1.0)

'FEEDBACK DETERMINATION'

    ERR = COS1**2+SIN1**2-1
    INTERR = INTEG(ERR,0.0)
    FC = ERR+INTERR

' *** TRANSMIT IF FILTER *** '

'@MINVAL TZETA1=0,TW1=100,TG1=0'
'@MAXVAL TZETA1=1,TW1=9.425E8,TG1=10'
'@SCALE    TSUM1=6,TSTAG1=2,TFEED1=2,TFLTIN=1'
CONSTANT TG1=1,TW1=.4398E9,TZETA1=.2143
LOGICAL FLT1IN

    TFLTIN = RSW(FLT1IN,TIF,SIN1)

    TSUM1=(TG1*2*TZETA1*TFLTIN - TSTAG1*2*TZETA1 - TFEED1)
                                 TSTAG1=INTEG(TSUM1*TW1,0)
```

```
        TFEED1=INTEG(TSTAG1*TW1,0)

'@MINVAL TZETA2=0,TW2=100,TG2=0'
'@MAXVAL TZETA2=1,TW2=9.425E8,TG2=10'
'@SCALE TSUM2=6,TSTAG2=2,TFEED2=2'
CONSTANT TG2=2.45,TW2=.365337E9,TZETA2=.105324

   TSUM2=(TG2*2*TZETA2*TSTAG1 - TSTAG2*2*TZETA2 - TFEED2)
   TSTAG2=INTEG(TSUM2*TW2,0)
   TFEED2=INTEG(TSTAG2*TW2,0)

'@MINVAL TZETA3=0,TW3=100,TG3=0'
'@MAXVAL TZETA3=1,TW3=9.425E8,TG3=10'
'@SCALE TSUM3=6,TSTAG3=2,TFEED3=2'
CONSTANT TG3=1.7,TW3=.529492E9,TZETA3=.105324

   TSUM3=(TG3*2*TZETA3*TSTAG2 - TSTAG3*2*TZETA3 - TFEED3)
   TSTAG3=INTEG(TSUM3*TW3,0)
   TFEED3=INTEG(TSTAG3*TW3,0)


LOGICAL FTYPE
'@SCALE RSTAG3=2'

   FILT = RSW(FTYPE,RSTAG3,TSTAG3)

'@SCALE P1=1,LSUM=4,LP1=1,LP2=1.1,PEAK=1.1,FPEAK=1.1'

   P1 = FILT*FILT
   LSUM = 2*P1 - 2*.707*LP1 - LP2
   LP1 = INTEG(LSUM*FRSWC,0)
   LP2 = INTEG(LP1*FRSWC,0)
   PEAK = SQRT(LP2)
   FPEAK =  PEAK + ZERO

'@SCALE IF=1,RIF=1'

   IF = 2*SCOEF*TSTAG3 + NCOEF*NOISE
   RIF = TRACK(IF,0,.FALSE.,.FALSE.)


   '@RECORD(REC01,,,,,,,,SINE ,TIBB,TQBB,...
                        RIF,SRSD2 ,FILT,TFLTIN,TSTAG3)'
   '@RECORD(REC02,,,,,,,,AD10I,AD10Q,LEVBUF,PEAK,QUAD,P1,...
                        TIF,RSTAG3)'
```

```
          'QEND PARALLEL'
        END
    END

    TERMINAL
    END
END
*TRANSLATE (6)

 TRNKOUT(1) = RIF,TGREY,SIN1
 TRNKIN(1)=RSTAG3

 DAM(1)=TGRAY,TGRDIF
 SL(1)=TCLOCK

 CONNECT AOT1E00=AAD10S,AOT1E01=SRSD2,AOT1E02=SRSD2,AOT1E03=SRSD2
 CONNECT AOT1E04=LEVBUF

 CONNECT AIT1E00=AD10I,AIT1E01=AD10Q, AIT1E02=NOISE
 PADC(1)=FPEAK
 DCA(1)=OMEGA,OMEGA,OMEGA,OMEGA

*OUTPUT(6)
*END
```

The following is a listing of the Fortran and assembly program used to implement the digital portion of the hybrid program.

```
C
C
      SUBROUTINE ZZSIML
C
C     CREATED 12/12/85 BY V.COSTANZA
C
         INCLUDE '@SYSTEM(PGSC00)S.ZZCOM'
         INCLUDE '@SYSTEM(PGSC00)S.ZZSIMC'

      IF(ZZI.NE.0)GOTO 99999

C     INITIALIZE SIMSTAR
      CALL ZZSIC
      CALL ZZIHYB

      GOTO 99993
99999 CALL ZZNTLG
      IF(ZZI.EQ.2)GOTO 99997
99998 CONTINUE

C     INITIALIZE RUNB
      CALL ZZIRUN

      CALL ZZNITS
99997 CALL ZZNITA

      ZZST=.FALSE.
      IF(ZZI.EQ.1) THEN
         CALL ZZSRUN
       ELSE
         CALL ZZCRUN
      END IF

C     BEGIN REAL-TIME AND START RUN
      CALL ZZGORT
      CALL ZZSTRT

C                                    LOOP      UNTIL      TERMINATION
```

```
      DO UNTIL (ZZST)
       IF(ZZMEFLG) CALL ZZMEXC
        CALL ZZBACK
         CALL QRPMUMI(MODE)
        IF(MODE.EQ.5) ZZST=.TRUE.
      END DO

C     PLOT FREQUENCY RESPONSE
      CALL ZZPLOT
C      STOP RUN
      CALL ZZSTOP

      CALL ZZTRUN

99996 CONTINUE

C     TERMINAL
99995 CALL ZZTERM

99993 CONTINUE
      RETURN
      END

      SUBROUTINE ZZIHYB

C@    CREATE QPR.SYM
C     OPTION 1+

C@    COMMON
C@    REAL TIMSCL,RB,BITPSM,STEP,PRSAMP,PRSSGN,EBNO,TINT
C@    REAL NTCNST=5.0,FRSWC,OMEGA

C@    INTEGER IBTPSM=1,NLEVEL,SHFREG,PRS,RANAND,PRSMSB
C@    INTEGER PRSLVL,MAXLVL,MSBMSK,INBUF0,INBUF1
C@    INTEGER DIFMSK

      INCLUDE 'QPR.COM'

      OPTION 1-
C@    ENDCREATE

      INCLUDE 'QPR.SYM'

      CALL QSPSP(1)

      LEVTCR(1)=2 ; LEVTCR(2)=-1 ! SET UP SYMBOL DAM TCR AND ARRAY
                                 CALL      QNDAMTCR(LEVTCR,1,-1)
```

C-8

```
      CALL QWBDACPR(LEVTCR,0,1,1,TDAMS,2)
      CALL QSDALOOP(LEVTCR)
      CALL QIDACP  (LEVTCR)

      RETURN
      END


      SUBROUTINE ZZIRUN

      INCLUDE 'QPR.SYM'

      CALL ZZMOD
      CALL ZZPROB1
      CALL ZZCOEF

      IBTPSM=BITPSM+.1 ! INTEGERIZE BITS PER SYMBOL
      MAXLVL=2**IBTPSM - 1 ! MAXIMUM LEVEL FOR GIVEN # OF BITS/SYMBOL

      SHFREG=123456789 ! INITIALIZE RANDOM BIT SHIFT REGISTER

      IF     ( IBTPSM .EQ. 1 ) THEN
         RANAND=X'1'
      ELSE IF( IBTPSM .EQ. 2 ) THEN
         RANAND=X'3'
      ELSE IF( IBTPSM .EQ. 3 ) THEN
         RANAND=X'7'
      END IF

      MSBMSK=2**( IBTPSM-1 )

      RANAND=4*RANAND    ! WILL BE USED IN FULLWORD INDEX MODE
      DIFMSK=4*MSBMSK    ! WILL BE USED IN FULLWORD INDEX MODE
                         ! FOR DIFFERENTIALLY ENCODING MSB.

      DO PRS=0,MAXLVL

         PRSMSB=IAND(PRS,MSBMSK)


         IF( PRSMSB .EQ. 0 ) THEN
            PRSSGN = -1
         ELSE
            PRSSGN = +1
         END IF
```

```fortran
      IF    ( IBTPSM .EQ. 1 ) THEN

         PRSAMP=1.

      ELSE IF( IBTPSM .EQ. 2 ) THEN

         PRSLVL=IAND(PRS,X'1')
         IF     ( PRSLVL .EQ. 0 ) THEN
            PRSAMP=1./3.
         ELSE IF( PRSLVL .EQ. 1 ) THEN
            PRSAMP=3./3.
         END IF

      ELSE IF( IBTPSM .EQ. 3 ) THEN

         PRSLVL=IAND(PRS,X'3')
         IF     ( PRSLVL .EQ. 0 ) THEN
            PRSAMP=1./7.
         ELSE IF( PRSLVL .EQ. 1 ) THEN
            PRSAMP=3./7.
         ELSE IF( PRSLVL .EQ. 3 ) THEN
            PRSAMP=5./7.
         ELSE IF( PRSLVL .EQ. 2 ) THEN
            PRSAMP=7./7.
         END IF

      END IF

      LEVARA(PRS)= PRSSGN*PRSAMP

      END DO

      RETURN
      END


      SUBROUTINE ZZMOD

      INCLUDE 'QPR.SYM'
      INCLUDE 'COM.BAN'
      INTEGER ANS1,ANS2,ANS3,ANS5

      CALL INIT2
      CALL INIT1

      IF(FLAG .EQ. 1) GOTO 48
```

```fortran
5      WRITE('UT',10)
10     FORMAT('      WHAT DO YOU WISH TO DO?',/,
      +       '        1 START  RUN',/,
      +       '        2 SPECIFY NEW RUN CONDITIONS',/,/,
      +       '        >')
       READ ('UT',1,ERR=5,END=5) ANS1
1      FORMAT(I1)

       IF(ANS1 .EQ. 2) THEN
15        WRITE('UT',20)
20        FORMAT('      WHAT DO YOU WANT TO CHANGE?',/,
      +          '        1 TRANSMITTER / RECEIVER',/,
      +          '        2 ENVIRONMENT',/,/,
      +          '        >')
          READ('UT',1,ERR=15,END=5) ANS2

       ELSE IF(ANS1 .EQ. 1) THEN
              GO TO 75
       ELSE
          GO TO 5
       END IF


          IF(ANS2 .EQ. 1) THEN
25           WRITE('UT',30)
30           FORMAT('      WHAT DO YOU WANT TO CHANGE?',/,
      +             '        1 BANDPASS FILTER MODELS',/,
      +             '        2 BITS PER SYMBOL',/,/,
      +             '        >')
             READ('UT',1,ERR=25,END=5) ANS3

             IF (ANS3 .EQ. 1) THEN
35              WRITE('UT',40)
40              FORMAT(' CHANGE THE BANDPASS FILTER IN THE:',/,
      +                '        1 TRANSMITTER',/,
      +                '        2 RECEIVER',/,
      +                '        3 BOTH TRANSMITTER AND RECEIVER',/,/,
      +                '        >')
                READ('UT',1,ERR=35,END=5) ANS4

          CALL ZZBAN
            IF(ANS.EQ.'Y') GOTO 75

48        CONTINUE
            ANS4=ANS4-1
          IF(ANS4.EQ.2) THEN
                                              CALL      ZZBAN
```

```
                IF(ANS.EQ.'Y') GOTO 75
          ELSE
           END IF


       FLAG=0

                ELSE IF (ANS3 .EQ. 2) THEN
45                 WRITE('UT',50)
50                 FORMAT('   ENTER 1,2, OR 3 BITS PER SYMBOL',/,/,
          +                    '   >')
                   READ('UT',*,ERR=45,END=5) BITPSM

                ELSE
                   GO TO 15
                END IF

            ELSE IF (ANS2 .EQ. 2) THEN

55              WRITE('UT',60)
60              FORMAT('     WHAT DO YOU WANT TO CHANGE?',/,
          +            '         1 EB/N0',/,
          +            '         2 MULTIPATHING',/,/,
          +            '         >')
                READ('UT',1,ERR=55,END=5) ANS5

                IF(ANS5 .EQ. 1) THEN

65                   WRITE('UT',70)
70                   FORMAT('  ENTER DESIRED EB/N0 IN DB',/,/,
          . +                '   >')
                     READ('UT',*,ERR=65,END=5) EBN0
                END IF

       ELSE
            GO TO 15
       END IF

       GO TO 5
75     WRITE('UT',80)
80     FORMAT('   * PROGRAM EXECUTING *')

       RETURN
       END
```

```
      SUBROUTINE ZZBACK

      INCLUDE 'QPR.SYM'
      INCLUDE '@SYSTEM(PGSC00)S.ZZCOM'
      INCLUDE 'COM.BAN'

      LOGICAL QRSLL

      INTEGER REGBUF(3),REG3

      CALL QSDAMTRA(LEVTCR) ! LOAD AND TRANSFER SYMBOL LEVEL DAM

  100 IF( .NOT.QRSLL(0) )GO TO 100 ! WAIT ON XMIT CLOCK PULSE

***********************************************************************
*                                                                     *
*     USE 32 BIT SHIFT REGISTER TO CREATE RANDOM BIT STREAM           *
*     REQUIRES FEEDBACK AND EXCLUSIVE-OR OF BITS 0,10,30,& 31.        *
*                                                                     *
***********************************************************************



      INLINE

      STF       5,REGBUF    BUFFER REGISTERS 5 THRU 7
      STW       3,REG       BUFFER REGISTER 3

      LNW       5,IBTPSM    LOAD THE NEG. VAL. OF # BITS/SYMBOL


      LW        7,SHFREG    LOAD SHIFT REGISTER CONTENTS

)555  ZR        6           ZERO REGISTER 6

      RND       6           IF BIT 31 OF SHFREG IS 1, INCR. REG 6

      SRC       7,1         MOVE BIT  0 OF SHFREG TO MSB
      RND       6           IF BIT  0 OF SHFREG IS 1, INCR. REG 6

      SRC       7,10        MOVE BIT 10 OF SHFREG TO MSB
      RND       6           IF BIT 10 OF SHFREG IS 1, INCR. REG 6

      SLC       7,12        MOVE BIT 30 OF SHFREG TO MSB
      RND       6           IF BIT 30 OF SHFREG IS 1, INCR. REG 6
```

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```
         SRC     7,1         MOVE BIT 31 OF SHFREG TO MSB

         SRLD    6,1         SHIFT SHFREG RIGHT ONE BIT AND MOVE THE
C                            LSB OF SUM OF HIGH BITS TESTED INTO THE
C                            MSB OF SHFREG. THIS IS EQUIVALENT TO
C                            EXCLUSIVE-ORING THE TESTED BITS AND PUTTING
C                            THE RESULT INTO THE MSB OF SHFREG.

         BIB     5,)555      INCREMENT LOOPCOUNTER & BRANCH IF NOT ZERO

         STW     7,SHFREG    STORE THE RESULT BACK INTO MEMORY

         ANMW    7,RANAND
         TRR     7,3         USE THE PRESENT WORD FOR A FULLWORD INDEX
         LW      6,LEVARA,3  TO GRAB A GRAY ENCODED LEVEL OUT OF ARRAY
         STW     6,GRAY      STORE LEVEL INTO D/A INPUT ARRAY
C                            IN GRAY ENCODED TRANSMIT SLOT.
C                            CORRESPONDS TO D/A #0.

         LW      7,INBUF1    GRAB 2ND LAST WORD FOR DIFFERENTIAL ENCODING
         ANMW    7,DIFMSK    MASK OFF THE MSB OF THE 2ND LAST WORD
         EOR     7,3         DIFFERENTIALLY ENCODE THE MSB OF THE WORD

         LW      6,INBUF0    SHIFT OLD INBUF0 TO INBUF1
         STW     6,INBUF1
         STW     3,INBUF0    STORE NEW INBUF0 THAT WAS JUST CREATED

         LW      6,LEVARA,3  TO GRAB A GRAY ENCODED LEVEL OUT OF ARRAY
         STW     6,DIFGRA    STORE LEVEL INTO D/A INPUT ARRAY
C                            IN DIFFERENTIALLY AND GRAY ENCODED TRANSMIT
C                            SLOT. CORRESPONDS TO D/A #1.

         LF      5,REGBUF    REFRESH USED REGISTERS
         LW      3,REG3      REFRESH USED INDEX REGISTER

         ENDI

C     FREQUENCY RESPONSE SET UP

      IF(ANS .EQ. 'N') GOTO 34
       IF(FCOUNT.EQ.0) NTCNST=10
      DELAY = NTCNST*1000*TIMSCL/FRSWC
      FCOUNT = FCOUNT + 1

      CALL WAIT(DELAY,1,KK)

                                          BUFF(FCOUNT)=QRPADC(0)
```

```fortran
      CALL WAIT(1,1,LL)
       IF(BUFF(FCOUNT).LT. .001) BUFF(FCOUNT)=.01
      MAG(FCOUNT) = 20*ALOG10(1.1*BUFF(FCOUNT))
      XAXIS(FCOUNT) = WI/6.28318E6
      WI =WI + DELTAW

      DO LL=1,2
       OMEG(LL)=WI/OMEGA
      END DO


      CALL QWBCOEF(LOGNUM,OMEG,2)
      CALL WAIT(50,1,NN)

7     CONTINUE
         IF(FCOUNT.EQ.(NPOINT)) ZZST=.TRUE.

34    CONTINUE
      RETURN
      END

        SUBROUTINE ZZBAN
          INCLUDE 'T1.QPR'
          INCLUDE 'COM.BAN'

        CHARACTER*8 FILTER
        REAL PII
        PII=3.14159
        I=0
        ORDER=6
        RIPPLE=0

        IF(ANS4.EQ.2) THEN
          FILTER='RECEIVE '
        ELSE
          FILTER='TRANSMIT'
        END IF

91      WRITE('UT',10) FILTER
10      FORMAT('          ENTER ',A8,' FILTER TYPE',/,
     +         '             1 CHEBYCHEV',/,
     +         '             2 BUTTERWORTH',/,
     +         '             3 BESSEL',/,
     +         '             >')
        READ('UT',3,ERR=91) FILTYP
3       FORMAT(I1)
```

```
19        WRITE('UT',9)
  9       FORMAT('  ENTER CENTER FREQUENCY AND BANDWIDTH IN Mhz > ')
          READ('UT',*,ERR=19) CNTFRQ,BNDWTH
999       FORMAT(F10.1)

          IF(FILTYP.EQ.1) THEN
          WRITE('UT',11)
 11       FORMAT('  ENTER PASSBAND RIPPLE IN DB > ')
          READ('UT',*) RIPPLE
          END IF

          WCTOT=2*PII * CNTFRQ * 1000000
          BWTOT=2*PII * BNDWTH * 1000000

          BQD1ST=0
          BQDNUM=BQD1ST
          NORDER=ORDER/2
            POLNUM=0


100       POLNUM=POLNUM + 1
          NLPPOL=NRMPOL(FILTYP,POLNUM,RIPPLE)
          BWPOL=BWTOT*NLPPOL

          IF ( AIMAG(NLPPOL).EQ.0 ) THEN
C
C            A PURE REAL POLE YIELDS ONE DENORMALIZED POLE PAIR
C
          DBPPOL=( BWPOL+CSQRT( BWPOL**2 - 4*WCTOT**2 ) )/ 2
          CALL SETBQD
          BQDNUM=BQNUM+1
C
C
          ELSE
C

C          A COMPLEX POLE YIELDS TWO DENORMALIZED POLE PAIRS

          DBPPOL=( BWPOL+CSQRT( BWPOL**2 - 4*WCTOT**2) )/ 2
            CALL SETBQD
            BQDNUM=BQDNUM+1
          DBPPOL=( BWPOL-CSQRT( BWPOL**2 - 4*WCTOT**2) )/ 2
            CALL SETBQD
            BQDNUM=BQDNUM+1

          END IF
                      IF( BQDNUM .LT. ( NORDER              ) ) THEN
```

```
            GO TO 100
        ELSE
        END IF
      RETURN
        END
C
C
      SUBROUTINE SETBQD
C
C     THIS SUBROUTINE SETS THE COEFFICIENTS TO THE PROPER
C     VALUES, SUCH THAT THE CENTER FREQUENCY AND GAIN
C     MATCH THOSE SPECIFIED BY THE LOCATION OF THE DENORMALIZED
C     BAND PASS POLE (DBPPOL), AND THE LOCAL BIQUAD GAIN
C     (DBPGAN) IS UNITY AT THE OVERALL FILTER CENTER FREQUENCY.
C
C
C     CALCULATE LOCAL CENTER FREQ, BANDWIDTH AND GAIN
C
      INCLUDE 'COM.BAN'
       I = I + 1
        WCLOC = CABS( DBPPOL )
        DBPGAN = -BWTOT*CABS(NLPPOL)/(2*REAL(DBPPOL))

        IF(ANS4.EQ. 1 .OR. ANS4.EQ.3) THEN
          CALL TFILT
        ELSE
          CALL RFILT
        END IF
      RETURN
       END

      SUBROUTINE TFILT

      INCLUDE 'COM.BAN'
      INCLUDE 'T1.QPR'
      INCLUDE 'E1.QPR'
       GO TO(10,20,30) I

10       TG1 = DBPGAN
         TW1 = WCLOC
         TZETA1 = -REAL(DBPPOL)/TW1
        RETURN
20       TG2 = DBPGAN
         TW2 = WCLOC
         TZETA2 = -REAL(DBPPOL)/TW2
        RETURN
```

```
30       TG3 = DBPGAN
         TW3 = WCLOC
         TZETA3 = -REAL(DBPPOL)/TW3

      CALL INTPLT
      IF(ANS.EQ.'Y') L:FLT1IN=.FALSE.

      L:FTYPE=.FALSE.
      CALL ZZPSPP1
      CALL ZZCOEF
      CALL QSRUN

      RETURN
        END
       SUBROUTINE RFILT

       INCLUDE 'COM.BAN'
       INCLUDE 'T2.QPR'
      INCLUDE 'E2.QPR'

        GO TO(40,50,60) I

40       RG1 = DBPGAN
         RW1 = WCLOC
         RZETA1 = -REAL(DBPPOL)/RW1
         RETURN
50       RG2 = DBPGAN
         RW2 = WCLOC
         RZETA2 = -REAL(DBPPOL)/RW2
         RETURN

60       RG3 = DBPGAN
         RW3 = WCLOC
         RZETA3 = -REAL(DBPPOL)/RW3

       CALL INTPLT


      CALL QSPSP(2)
       IF(ANS.EQ.'Y') L:FLT2IN=.FALSE.
       CALL ZZPSPP1
       CALL ZZCOEF
      CALL QSPSP(1)

       RETURN
       END
```

```
      SUBROUTINE INIT1

      INCLUDE 'E1.QPR'
      INCLUDE 'COM.BAN'
      CALL QSPSP(1)
      L:FLT1IN=.TRUE.
      L:FTYPE=.TRUE.
      ANS='N'

      RETURN
      END

      SUBROUTINE INIT2

      INCLUDE 'E2.QPR'
      CALL QSPSP(2)
      L:FLT2IN=.TRUE.

      RETURN
      END

      SUBROUTINE INTPLT
      INCLUDE 'COM.BAN'
      INCLUDE 'T1.QPR'


      FCOUNT=0
      DELTAW = 0.0
      NPOINT=200
77    WRITE('UT',14)
      ANS='N'
14    FORMAT('  DO YOU WANT A FREQUENCY RESPONSE PLOT ? (Y or N) > ')
      READ('UT',3,ERR=77) ANS
3     FORMAT(A)
      IF(ANS.EQ.'N') GOTO 12
      IF(ANS4.EQ.3) FLAG=1
88    WRITE('UT',17)
17    FORMAT('  ENTER BEGINNING AND END FREQUENCIES IN Mhz > ')
      READ('UT',*,ERR=88) FREQ1,FREQ2

      WSTRT = FREQ1*6.283*1000000
      WSTOP = FREQ2*6.283*1000000

888   WRITE('UT',18)
18    FORMAT('  INPUT NUMBER OF PLOT POINTS (MAX=200) >')
      READ('UT',998,ERR=888) NPOINT
      998                                          FORMAT(I3)
```

```fortran
      IF(NPOINT.GT.200) GOTO 888

      DELTAW = (WSTOP-WSTRT)/NPOINT
      WI = WSTRT

      DO K=1,2
      OMEG(K)=WI/OMEGA
      LOGNUM(K)=K-1
      END DO

      CALL QWBCOEF(LOGNUM,OMEG,2)

12    RETURN
C
      END

      SUBROUTINE ZZPLOT

      CHARACTER*8 FIL
      INCLUDE 'COM.BAN'
      IF(ANS.EQ.'N') GOTO 31
      MAG(0) = NPOINT
      XAXIS(0) = NPOINT
      CALL INITT(960)
      CALL BINITT
      CALL CHECK(XAXIS(0),MAG(0))
      CALL DSPLAY(XAXIS(0),MAG(0))

       IF(ANS4.EQ.1 .OR. ANS4.EQ.3) THEN
         FIL='TRANSMIT'
       ELSE
         FIL='RECEIVE '
       END IF

      ENCODE(41,100,COMENT) FIL
100   FORMAT('FREQUENCY RESPONSE FOR ',A8,' IF FILTER')
      CALL WRITEK(200,720,41,0)

      ENCODE(12,300,COMENT)
300   FORMAT('MAGNITUDE DB')
      CALL WRITEK(0,600,12,1)

      ENCODE(15,200,COMENT)
200   FORMAT('FREQUENCY (MHZ)')
      CALL WRITEK(407,23,15,0)
```

```
          CALL FINITT(0,760)

   31     CONTINUE
          RETURN
          END

          SUBROUTINE WRITEK(XCOORD,YCOORD,NCHARS,VERHRZ)

C         THIS ROUTINE MOVES THE CURSOR ON THE TEK: TO THE X,Y
C         COORDINATES (XCOORD,YCOORD) ,THEN DISPLAYS THE FIRST
C         NCHARS CHARACTERS FROM THE ARRAY 'COMENT'. IF VERHRZ=1,
C         THE CURSOR WILL DISPLAY A VERTICAL COLUMN OF CHARACTERS
C          , OTHERWISE A HORIZONTAL ROW OF CHARACTERS WILL BE PRODUCED.

          INCLUDE 'COM.BAN'
          INTEGER CHRTCR,XO,YO,NO,XCOORD,YCOORD,NCHARS,VERHRZ
          INTEGER REG3,REG7

          NO=NCHARS
          XO=XCOORD
          YO=YCOORD

          IF(NO .GT. 80) NO=80

          DO 100 M=1,NO
          CHRCTR=0
            INDEX=M-1

          INLINE

            STW     7,REG7          STORE REGISTER 7 VALUE
            STW     3,REG3          STORE REGISTER 3 VALUE
            LW      3,INDEX         LOAD REGISTER 3 WITH BYTE LOCATION
            LB      7,COMENT,3      LOAD BYTE FROM COMENT TO REGISTER 7
            STW     7,CHRCTR        STORE RESULT IN CHRCTR
            LW      7,REG7          REPLACE REGISTER 7 WITH PREVIOUS VALUE
            LW      3,REG3          REPLACE REGISTER 3 WITH PREVIOUS VALUE

          ENDI

          CALL NOTATE(XO,YO,1,CHRCTR)

          IF(VERHRZ .EQ. 1) THEN
              YO = YO - 23
          ELSE
              XO = XO + 15
                                                      END         IF
```

END

DTIC

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END

DTIC

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